Outline

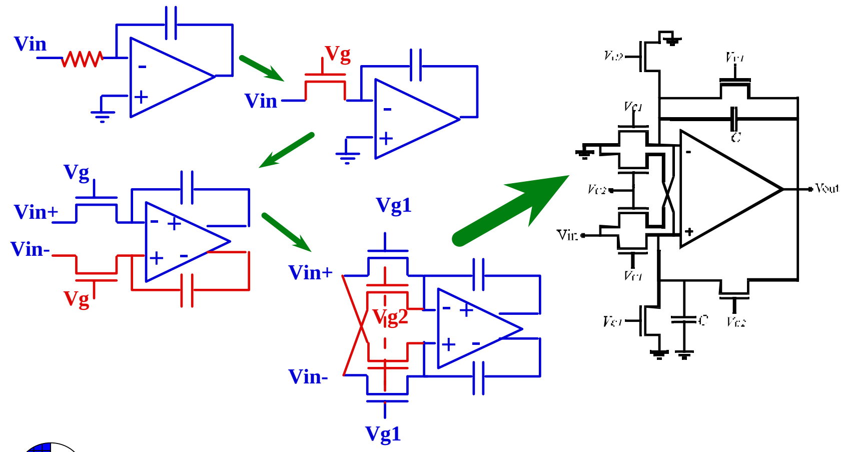
1/2. Analog design & Process assessment with Gm/Id
3. Output conductance (Vea), intrinsic capacitances
4. OTA design for low-voltage low-power applications

5. Harmonic distortion: MOSFET-C filters

+ Switches: SC - ADC
+ Bandgap / voltage references
+ Microsystems

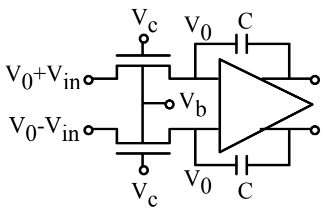
Filters

First-Order Mosfet-C Continuous time filter



Filters

Continuous-time MOSFET-C



R → MOS (R_{on} ÷ V_c, V_0)

↓ **$V_{in} = A.\sin(\omega.t)$**

(bulk) I_D ÷ V_{in}, V_{in}^2, $V_{in}^{3/2}$

⇓

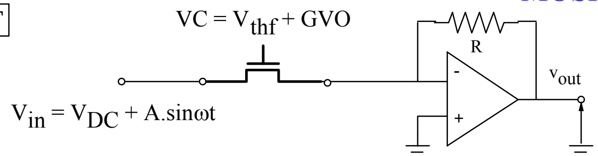
Harmonic distorsion (odd ÷ γ)

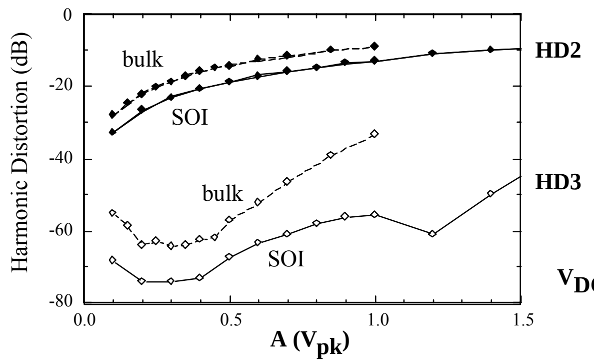
best candidate for low-voltage low-power continuous-time filter implementations with optimal dynamic range

SOI ?

MOSFET-C Filters

1-T



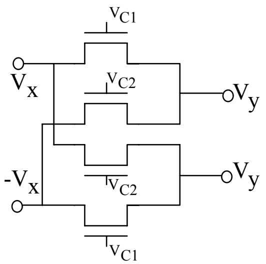


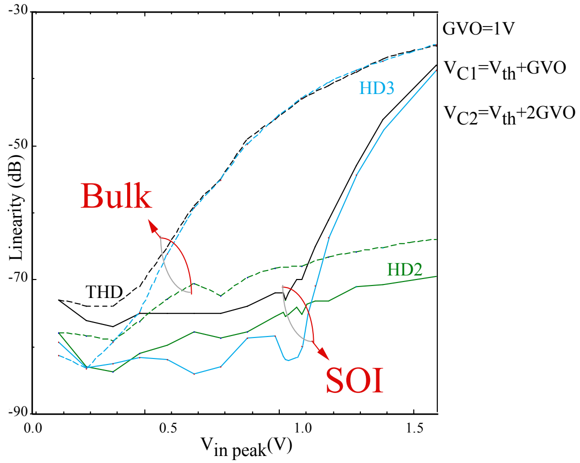
GVO = 1 V

V_{DC} = 0 V, SOI
1 V, bulk

MOSFET-C Filters

4-MOSFET structure





HD3 lower than 2-MOS
HD3 lower in FD SOI

MOSFET-C Filters

First-order realization

Frequency response of the filter (influence of Temperature)

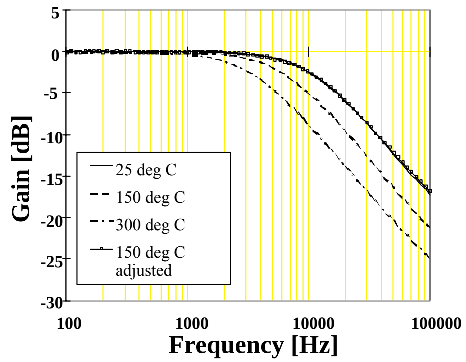
The increase of the Temperature lowers the mobility

↓

The equivalent MOS resistor increases

↓

On-Chip automatic tuning to compensate pole variations



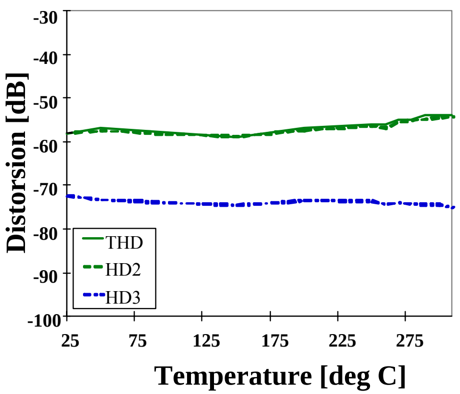
MOSFET-C Filters

Harmonic distorsion of the filter (influence of Temperature)

THD dominated by HD2

↓

Fully differential architecture to eliminate even order distorsion



Outline

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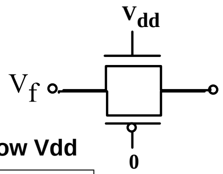
\+ Bandgap / voltage references
\+ Microsystems

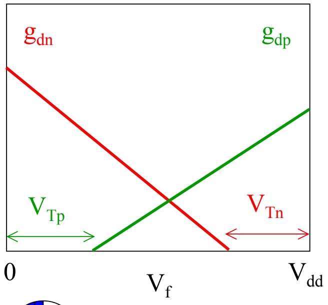
CMOS analog switch

Lowest V_{dd} for analog :



$$V_f \text{ if } V_{dd} > \frac{V_{Tp} \cdot n_n + V_{Tn} \cdot n_p}{n_p + n_n - n_p \cdot n_n}$$

Gap problem for low Vdd

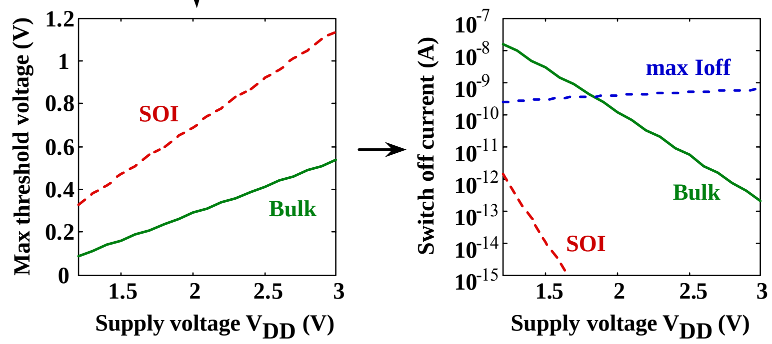


	n□ □	V_T	$V_{dd,min}$
Bulk	1.5	0.7	3.0
SOI	1.1	0.7	1.7
	1.1	0.4	1.0

CMOS analog switch

min device size + Ron < 50 kΩ

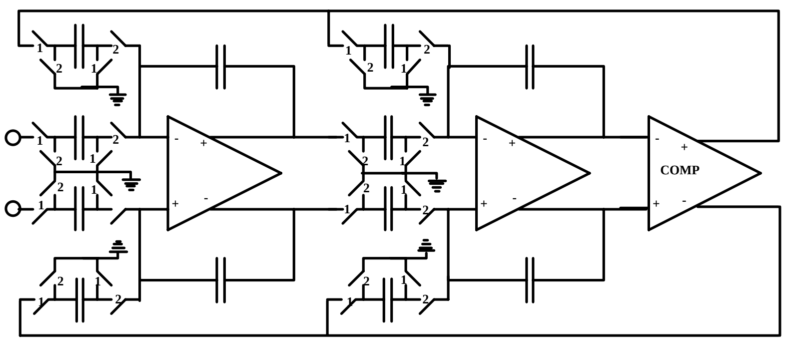
(settling error - 0.01% for 500 kHz and 2 pF)



min VDD

Switch applications

Second-order Sigma-Delta A/D Modulator



Architecture

Switch applications

Second-order Sigma-Delta A/D Modulator

Temperature	**30-250 °C**	**300 °C**
Sampling Frequency	**1 MHz**	**1 MHz**
OSR	**64**	**64**
Dynamic Range	**11 bits @30°C**	
	10 bits @250°C	**9 bits**
Peak SNR	**55 dB at RT**	**30 dB**
Supply Voltage	**5 V**	**5 V**

Measurement results

Outline

1. Analog design and Process assessment with Gm/Id
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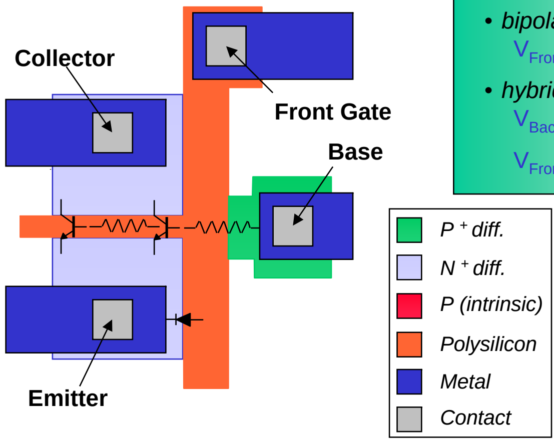
6. Bandgap / voltage references
   ULP circuit techniques: diodes, charge-pump

+ Microsystems

SOI lateral bipolar transistor

Structure



8µm x 1µm

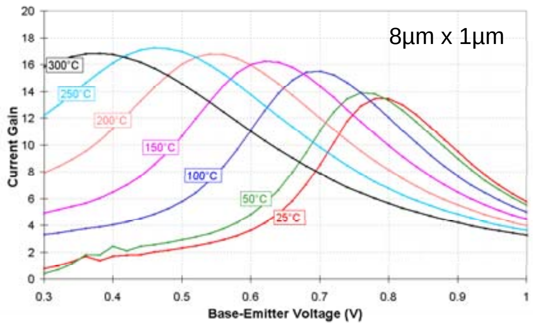
Two configurations :

- *bipolar mode* : $V_{Front\ Gate} = V_{Back\ Gate} = 0$ V
- *hybrid mode (BCG)* : $V_{Back\ Gate} = 0$ V, $V_{Front\ Gate} = V_{Body}$

SOI lateral bipolar transistor

Performances

Current gain from 25°C to 300°C

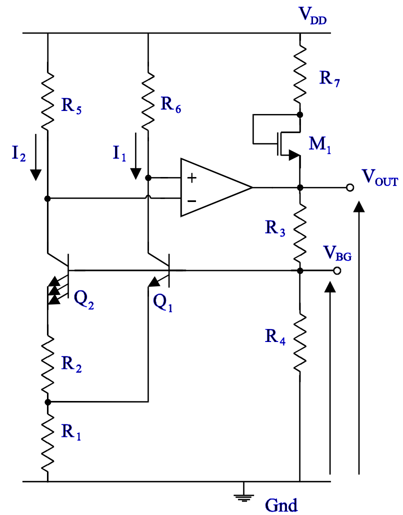


- *Current Gain* : 13 @ 25°C
  17 @ 300°C
- *Early Voltage* :10…20V
- *Base resistance* : 3…5kΩ
- *Good temperature linearity of V_{BE}* (slope : -1…-1.5mV/°C)

SOI lateral bipolar transistor

Bandgap circuit design

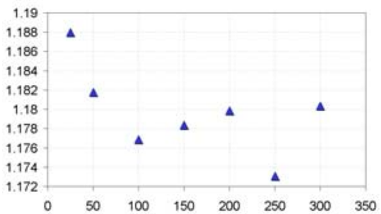
- $V_{bandgap} = V_{BE} + V_{PTAT}$
- *Design based on measurements*
- *single-stage OTA : negative feedback*
- *Supply Voltage : 4V to 5V*
- *Output Voltages : 1.2V & 3V*



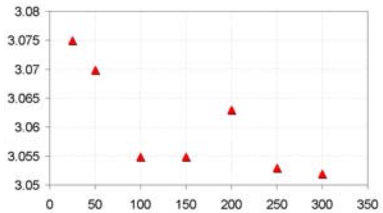
SOI lateral bipolar transistor

Experimental results

Bandgap voltage vs. T°



Reference voltage vs. T°



- max. 200 ppm/°C
- V_{BG} = 1.2V ± 130mV
- max. 98 ppm/°C
- V_{REF} = 3V ± 160mV

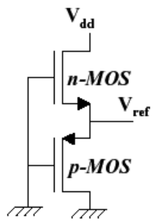
I_{cons} = 200µA Area = 0.385mm²

Fairly stable voltage over a very wide temperature range

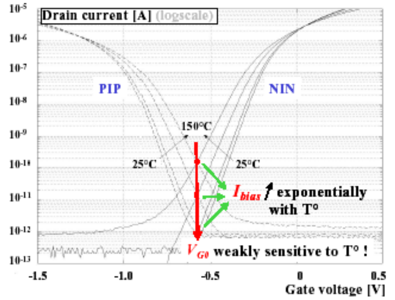
Voltage reference

A new Ultra-Low-Power (ULP) circuit

With low Vth devices



ULP voltage reference architecture.
(patented)



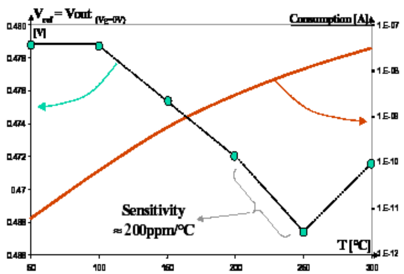
(log) IdVg curves for intrinsic FD SOI n- and p-MOSFETs over temperature.

… also for new diode, SRAM, charge-pumps concepts with ultra low leakage !

Voltage reference

New Ultra-Low-Power (ULP) circuit

Low Vth MOS implementation vs bipolar bandgap



Measured reference voltage and current consumption over temperature. (2µm) FD-SOI CMOS process, intrinsic n- and p-MOSFETs.

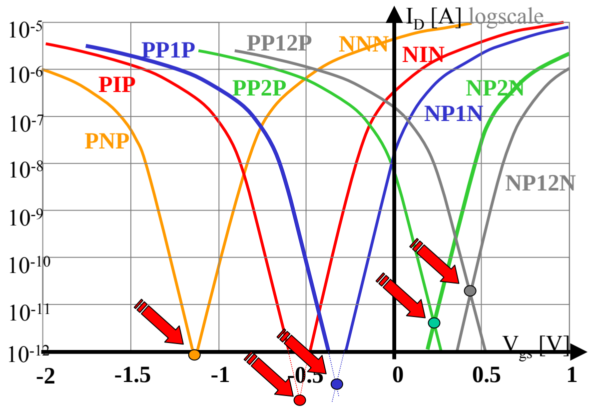
	ULP volt. ref	Bandgap [1]
Operating T°	25…300°C	25…300°C
Vdd-Vss	>0.6V	4…5V
Current consumpt.	1p…20nA (300°C)	200µA
Output voltage	0.47V (NIN-PIP)	3V ±160mV
Output drift	200ppm/°C	100ppm/°C
Active chip area	0.002mm²	0.385mm²

Performances comparison between the ULP voltage reference and a bandgap circuit.

Voltage reference

Other V_{ref} with multiple-V_{th} process

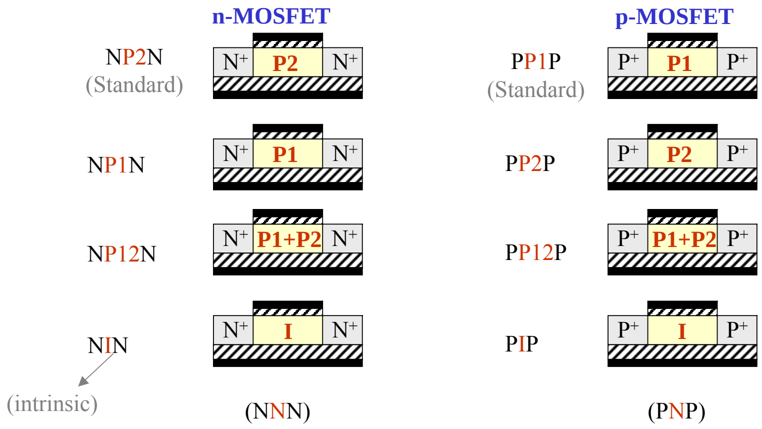
Id-Vgs characteristics after optimal doping mask use
(UCL FD-SOI process, V_{bs}=0V, 20°C, Vds=1V, W/L=1/3)



Multi-Vth

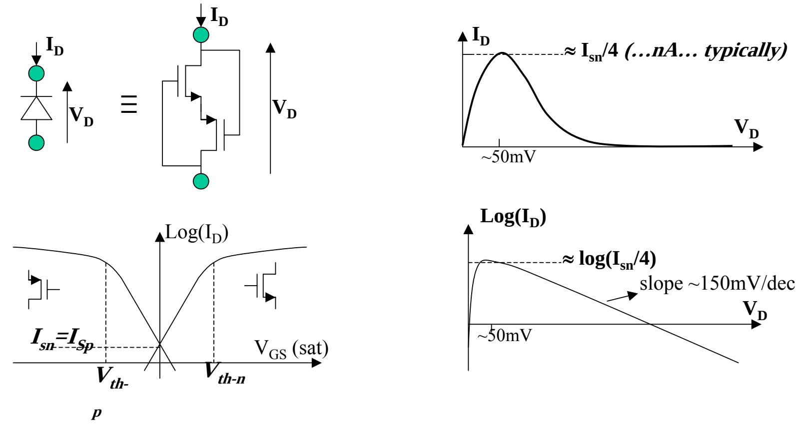
More V_{th} without process change ? …

Idea: Permute/Add/Remove channel doping by intelligent use of existing masks.



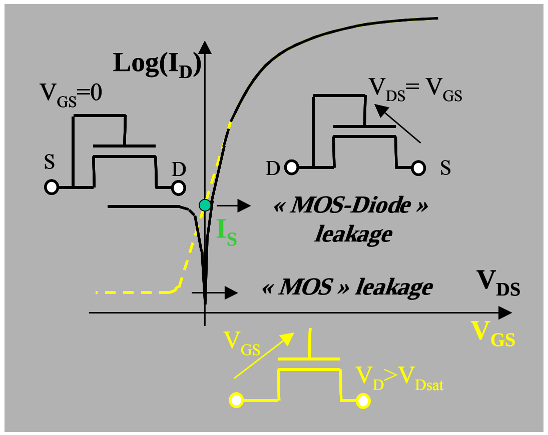
ULP circuit techniques

Reverse ULP diode



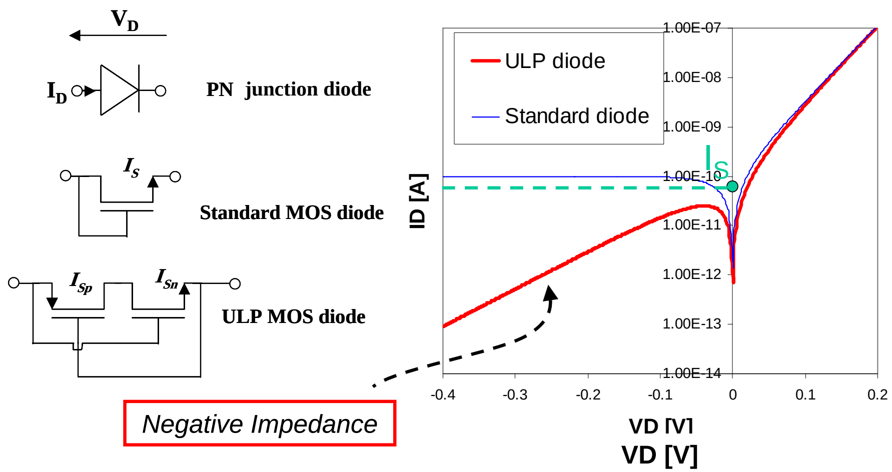
ULP circuit techniques

Classical MOS Diode

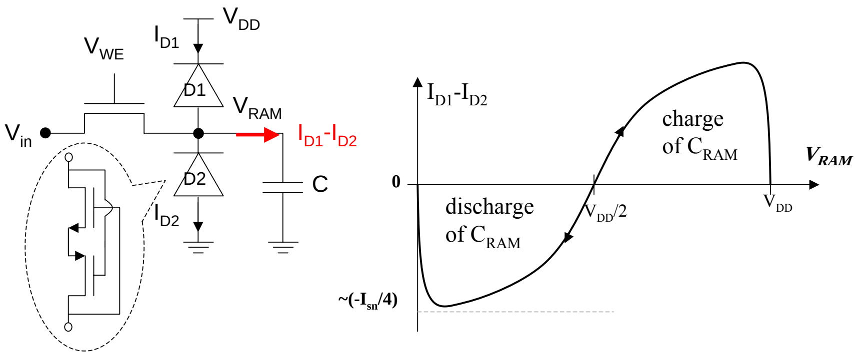


Large reverse leakage current for low V_{th} !

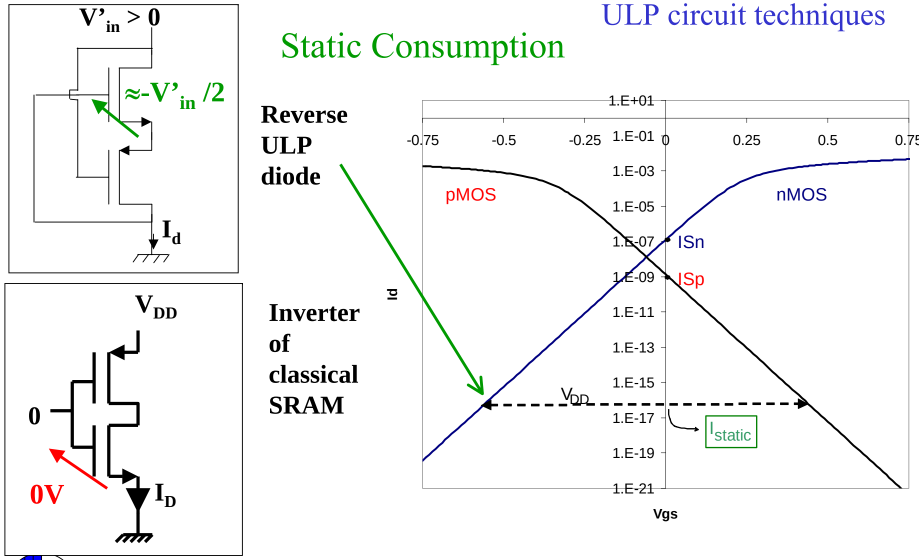
ULP circuit techniques



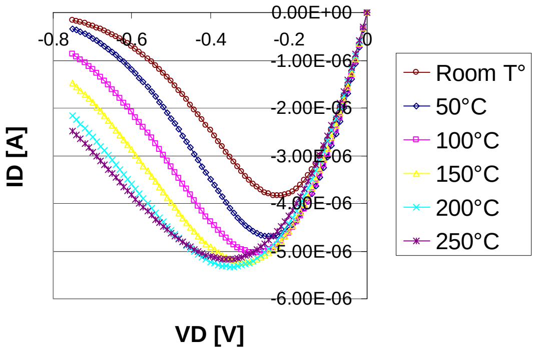
ULP Memory Cell



Static Consumption

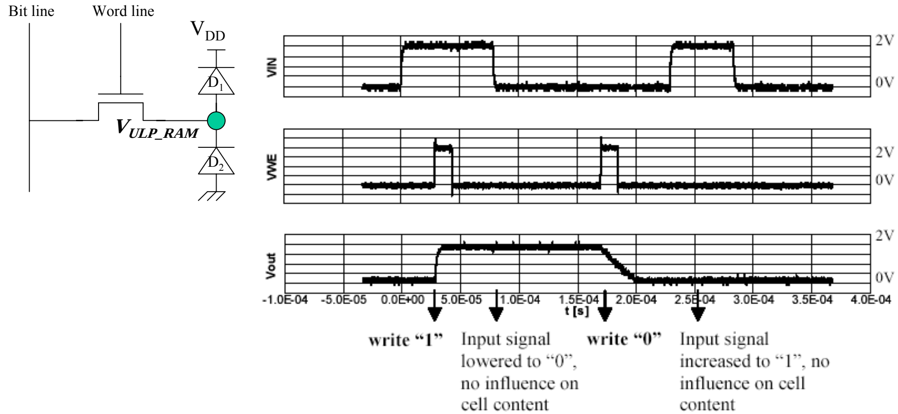


High Temperature Behavior



I-V characteristics of a ULP diode featuring NIN n-MOSFETs and PP12P p-MOSFETs with W=9µm and L=2µm

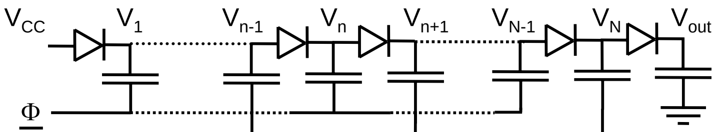
ULP Memory Functionality up to 280°C



Diode applications

Charge pump

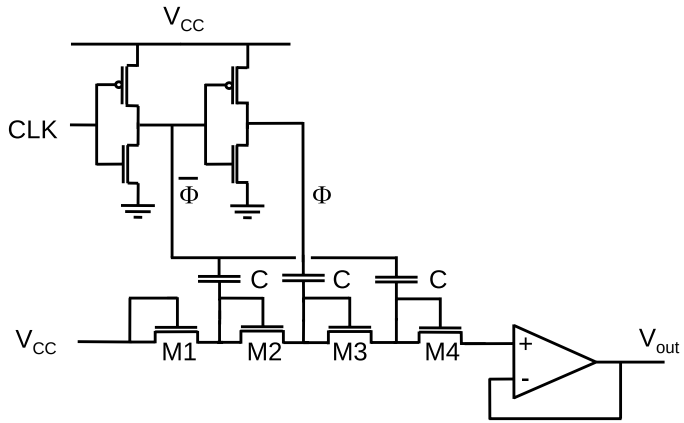
- Based on Dickson's



$$\text{Final voltage} = \text{supply voltage} + \left[N \times f\left(\frac{\Phi - V_D}{\lambda}\right) \right]$$

Charge-pump

- Design of 3x with MOS



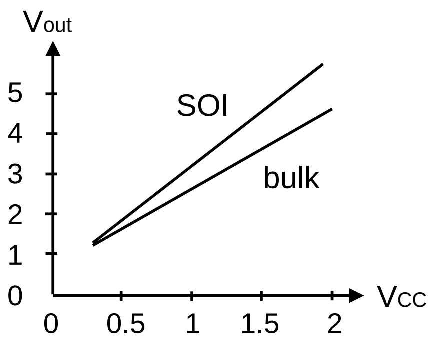
Charge-pump

- Specification :
  - » Supply Voltage = 1.8 V
  - » Programming voltage = 5 V
- SOI vs. bulk

Body effect

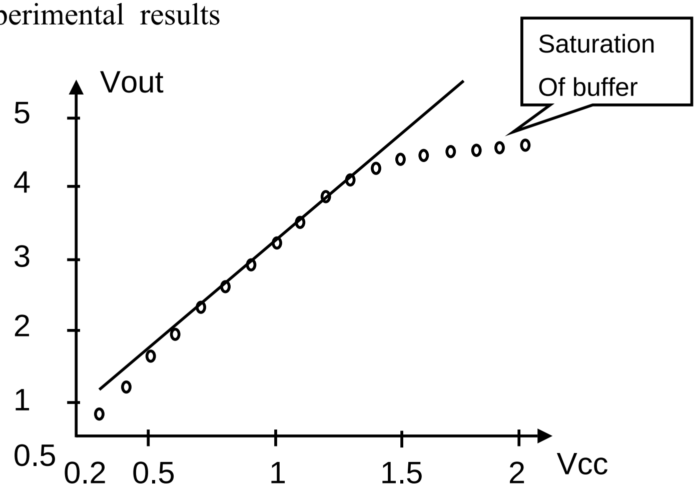
$n_{SOI} = 1.1$

$n_{bulk} = 1.5$



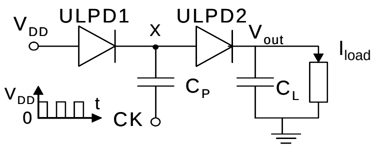
Charge-pump

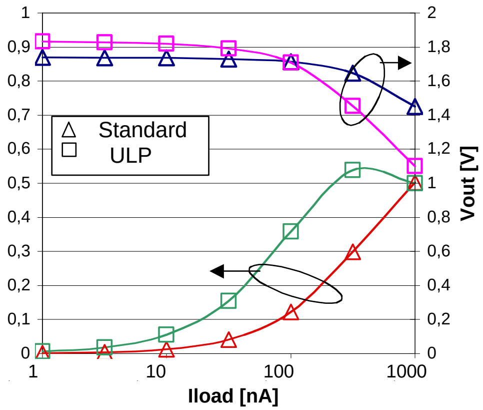
- Experimental results



Charge-pump

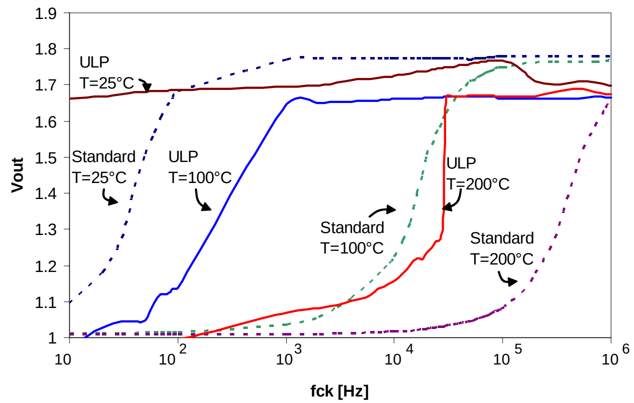
Voltage doubler with standard MOS and ULP diodes





Charge-pump

High-temperature behavior



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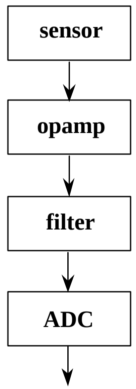
7. Heterogeneous microsystems

Microsystems

Towards fully integrated sensing chain…



High-gain(100dB), high-frequency (100MHz), low-noise…
⇒Very precise and stable instrumentation amplifiers

Continuous-time (RC active), Switched-cap
⇒Very linear

Sigma-delta (DR : 10 bits up to 250°C, 9 bits at 350°C)

…< 1.5-2 V

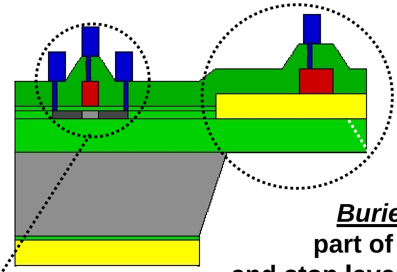
digital + memory

Ultra-low-power SRAM

… at 300-350°C

Smart SOI sensor

Electronics

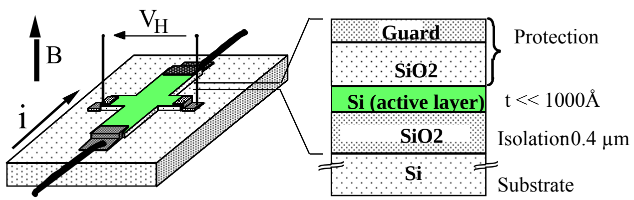


Sensor

Buried oxide **as part of a membrane and stop layer for silicon etching**
+
Specific sensitive layers

Silicon film **for proximity electronics and thin-film semiconductor sensors (T, B, UV) suitable to work in harsh environment: remote, high-temp., radiations…**

Development of a SOI based Hall Effect sensoR fOr an electricity meter



K_H = 100 V/(A.T)
S_T < 1000 ppm/K
R_c = 5 kOhm
Bruit = 1 µT/ √ Hz (1Hz), 300 nT/ √ Hz (> 1kHz)

Precision ≈ 0.2 %
DR = 1:2000

Objective: process compatibility for CMOS SOI and Hall cell / electronic circuit towards monolithic integration

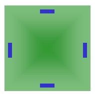
EUREKA project:
- Schlumberger Industries (Coordinator) - France
- Université de Montpellier II - France
- Ecole Polytechnique Fédérale de Lausanne (EPFL) - Switzerland
- LETI - France
- Microélectronique Marin (EMMARIN) - Switzerland
- Université catholique de Louvain-la-Neuve (UCL) - Belgium
- Crouzet Automatismes - France

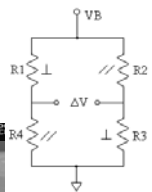
Bulk micromachining

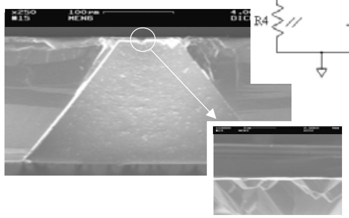
Si etch with TMAH *ou Tetramethylammonium hydroxyde*

On standard SOI wafers => Sandwich: 1 µm SiO_2 / Si_3N_4 LPCVD / SiO_2 PECVD

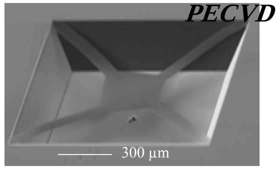
Differential Piezoresistive structure



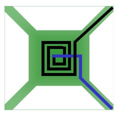


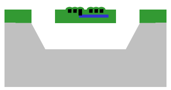


L = 100µm
e = 1µm
P_{max} = 5KPa

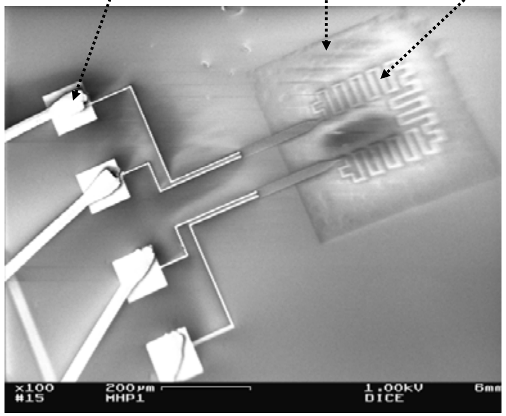


High Quality Factor inductors





4 contacts *membrane* *Polysilicon loop shape*



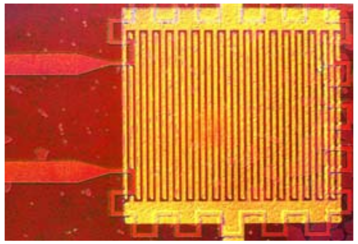
- ✓ **low cost**
- ✓ **very low consumption (20 mW at 400°C)**
- ✓ **high insulation (20.000 °C/W)**
- ✓ **high thermal uniformity**

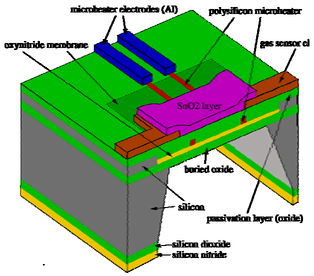
Applications : Gas, Flow, IR sensors...

Microsystems

The resistivity of a sensitive layer (as SnO_2 or WO_3) changes in presence of gases at 250 - 350°C

Microheater + interdigitated Au electrodes + sensitive layer



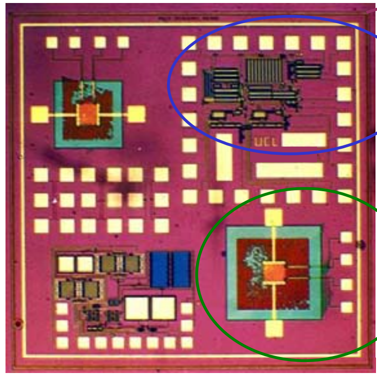


Microsystems

Co-integration of CMOS circuits and sensors, in compatible technologies, on same Si die

Goals: compacity, cost, performance

Example processed in UCL (DICE):



CMOS on silicon on insulator:
- analog circuits : Micropower, RF (1 GHz), Or High temperature (300-350°C)
- sensors: temperature, magnetic (Hall effect), optical (UV)

Sensors on membranes:
- Gas
- Pressure
- Flow
- Thermopiles (IR)…

Conclusion

- ***Generic High-performance Fully-Depleted SOI CMOS***
- ***Easy integration of special devices, sensors, MEMS***
- ***Operation in harsh conditions (micropower, high-temperature, remote RF link…)***
- ***Broad applications: automotive, aerospace, wireless sensors, biomedical, quality control…***
- ***« Green energy » or « Energy scavenging »: autonomy***