UCL Université catholique de Louvain

Analog design with Gm/Id in bulk and SOI CMOS

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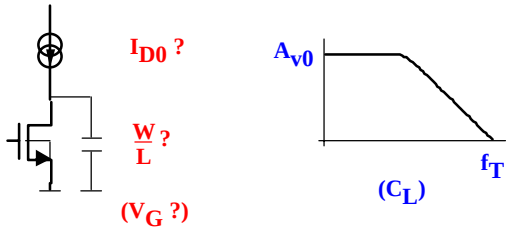
Synthesis ?

Intrinsic Gain Stage

unknowns *specifications*



Synthesis Problem

SPICE-like approach

inputs : W, L, V_G … → simulations → f_T, A_V, ϕ_m …

optimizer (starting point ?)

"Hand" estimation

specifications → small-signal circuit model → g_m, g_d … → device model → sizing

efficiency ÷ complexity of circuit and device models

Systematic approach

hand estimations + numerical tool (MATLAB) + g_m/I_D model or measure

Outline

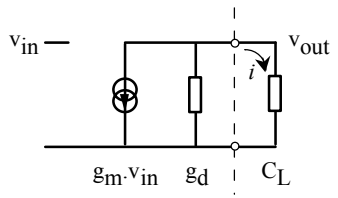
1. Small-signal approach / modelling

2. Process assessment of analog performance with Gm/Id
   - Definitions, Modelling
   - SOI vs bulk

3. Output conductance (Vea),Intrinsic capacitances, Mismatch…

4. Single-stage OTA design

Small-signal approach / modelling

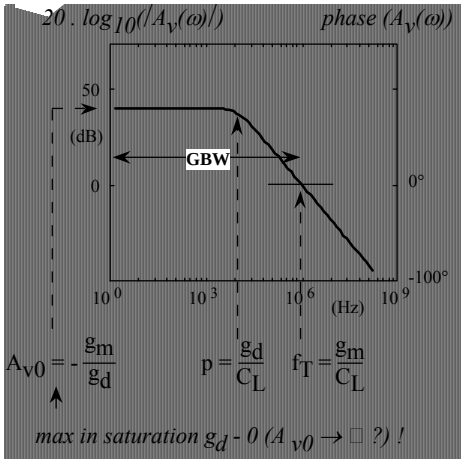


$i = j.\omega.C_L = - g_m.v_{in} - g_d.v_{out} \Rightarrow A_v = - \frac{g_m}{g_d + j.\omega.C_L}$

$I_D = \mu.C_{ox}.\frac{W}{L}.\frac{(V_G - V_{th})^2}{2.n}$ *in saturation*

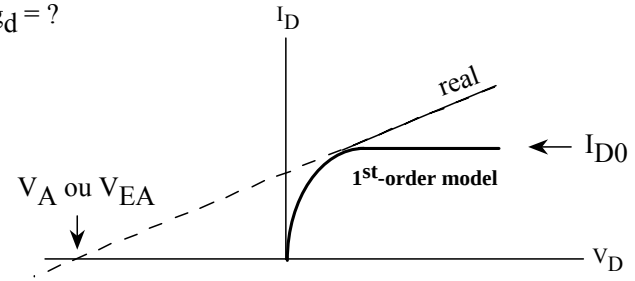
$g_m = \frac{\check{Z}\, I_D}{\check{Z}\, V_G}$ $\quad \mu.C_{ox}.\frac{W}{L}.\frac{V_G - V_{th}}{n}$ $= \beta.\frac{V_G - V_{th}}{n} = \sqrt{\frac{2.\beta.I_D}{n}}$

$g_d = \frac{\check{Z}\, I_D}{\check{Z}\, V_D}$ $\quad - 0$



Small-signal approach / modelling

$g_d = ?$



(V_{EA} - 20…30 V for L = 2…3 µm)

$g_d - I_{D0} / V_{EA} \quad \Rightarrow \quad A_{v0} = - \frac{g_m}{I_{D0}} . V_{EA}$

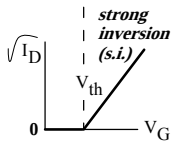
V_{EA} ($=I_d/g_d$) is preferred to g_d to avoid dependence on I_d

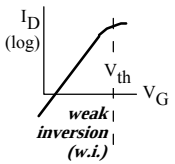
Small-signal approach / modelling

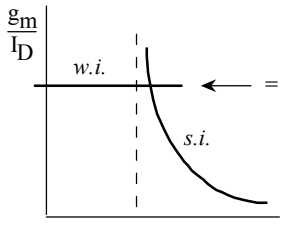
g_m / I_D ?

in saturation : $\frac{g_m}{I_D} = \frac{2}{V_G - V_{th}} = \sqrt{\frac{2.\beta}{n.I_D}}$ $\quad \beta = \mu.C_{ox}.\frac{W}{L}$

(does not depend on MOS sizes, only on inversion degree !) ⟶ **I' = I_D / (W/L)**



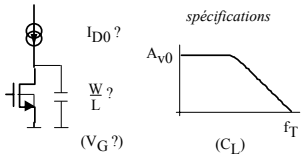




$= \frac{1}{I_D}.\frac{\check{Z}\, I_D}{\check{Z}\, V_G} = \frac{\check{Z}\, ln\,(I_D)}{\check{Z}\, V_G} = \frac{1}{n.U_T}$

(U_T = k.T/q - 26 mV at RT°, ⇒ theoretical max. - 38 V^{-1})

Small-signal approach / modelling

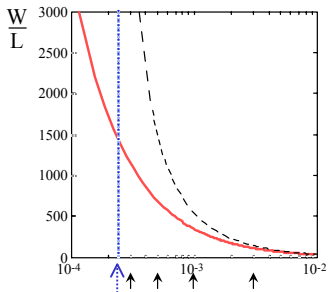


1) Strong Inversion

$g_m = 2.\check{s}\,.\,f_T\,.\,C_L$ &

$g_m = \sqrt{\frac{2.\beta.I_D}{n}} \Rightarrow$

$\frac{W}{L} = \frac{n.(\omega_T\,.\,C_L)^2}{2.\mu.C_{ox}.I_{D0}}$



f_T = 100 MHz

C_L = 10 pF

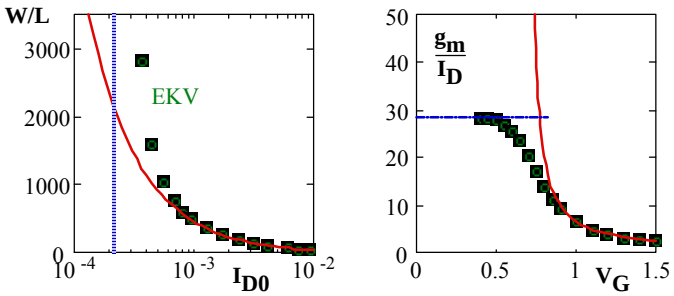
$\mu.C_{ox}$ = 57 µA/V^2

g_m/I_{D0} =	21,	12,	6,	2 V^{-1}	
A_{v0} =	52,	47,	41,	32 dB	(V_{EA} = 20 V)
V_G =	0.83,	0.96,	1.13,	2.5 V	(V_{th} = 0.9 V)

2) Weak Inversion

$g_{m,max} = I_D/(n.U_T)$ => $I_D = n.U_T.\omega_T.C_L$

Small-signal approach / modelling



EKV model

$$g_m / I_D = \frac{1}{n.U_T} . \frac{(1 - e^{(-\sqrt{IC})})}{\sqrt{IC}} \quad \textit{with} \quad IC = \frac{I_D}{2.n.\mu.C_{ox}.\frac{W}{L}.U_T^2}$$

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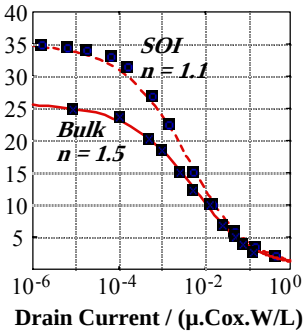
SOI vs Bulk 2 µm MOSFETs

Transconductance / Current Ratio (1/V)



$$g_m/I_D \xrightarrow{w.i.} 1/(n.U_T) \qquad g_m/I_D \xrightarrow{s.i.} \sqrt{\frac{2.\mu.Cox.W/L}{n.I_D}}$$

experimental data

EKV model (EPFL)

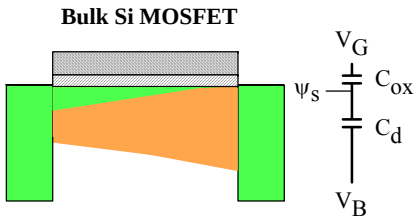
↳ ***n* factor**

÷ gate/substrate coupling (i.e. S in w.i. γ in s.i.)

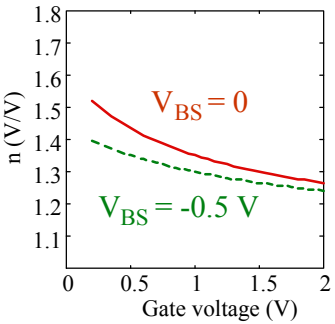
Body effect !

Gm/Id assessment

Body effect in bulk/PD MOSFET



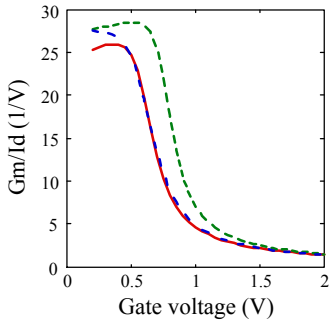
$$n = 1 + \frac{C_d}{C_{ox}} = f(V_{GB})$$

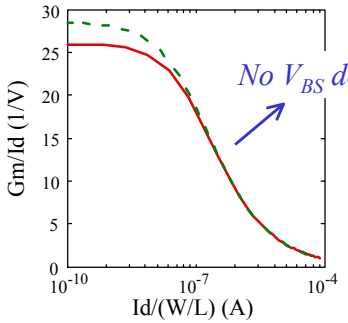


Gm/Id assessment

$n = f(V_{GB})$ @ $V_{BS} = 0$, $n = f(V_{GB})$ @ $V_{BS} = -0.5$ V

n = constant = 1.4

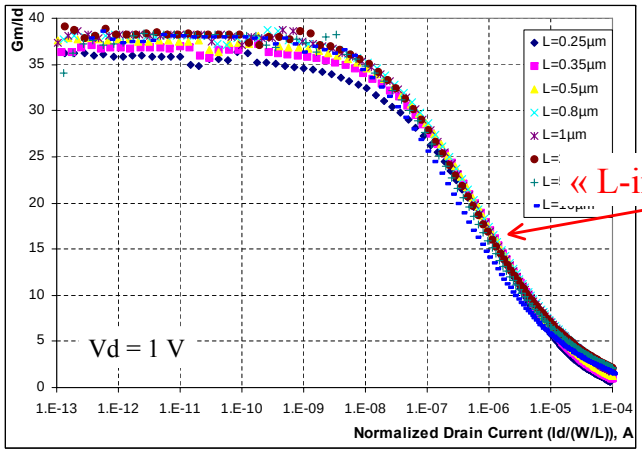




No V_{BS} dependence

Constant « n » value: OK as first-order evaluation

0.25 µm FD SOI MOSFETs



« L-independence »

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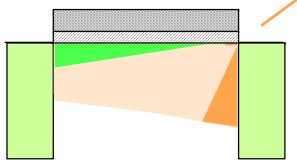
Early voltage

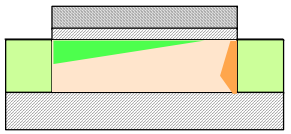
V_{EA} ($=I_d/g_d$) is preferred to g_d to avoid dependence on I_d

Bulk Si MOSFET

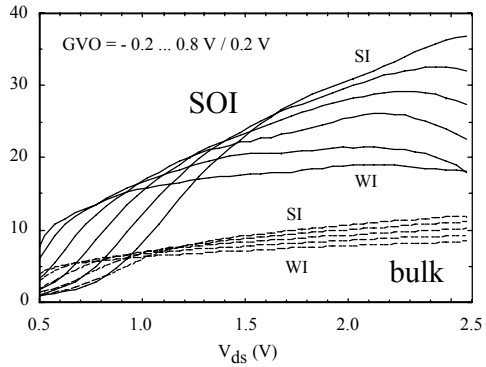


Depends on drain depletion penetration

SOI MOSFET

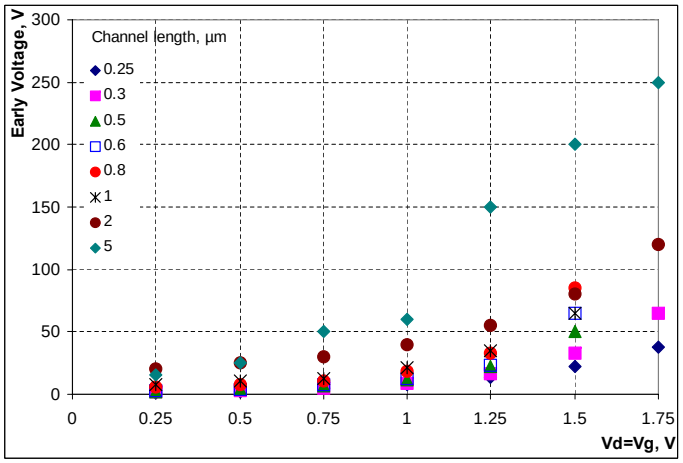


V_{EA} (V) in 2µm bulk and FD processes



Early voltage

Similar L and V dependencies in 0.25 µm processes: ≈ 10 V/µm_L

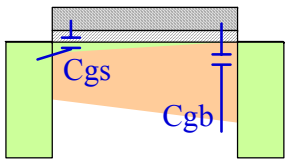


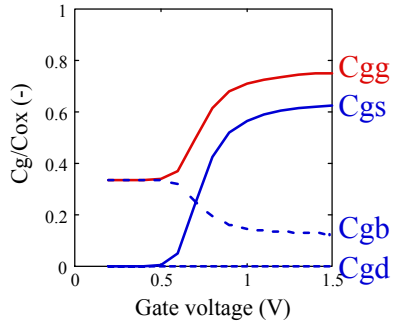
Intrinsic gate capacitances

$$C_{ij} = \pm \frac{\partial Q_i}{\partial V_j}$$

In saturation:

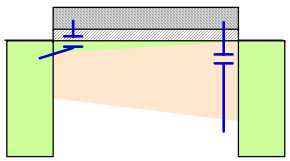
Bulk Si MOSFET



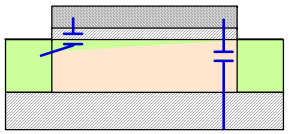


Intrinsic gate capacitances

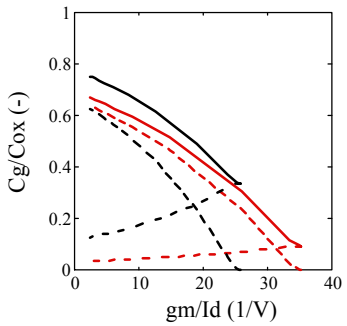
Bulk Si MOSFET



FD SOI MOSFET



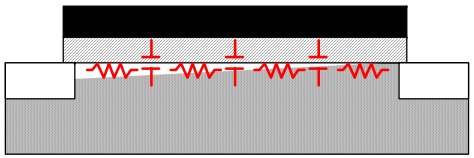
Cgs (---), Cgb (-.-), Cgg (___)



Cg smaller in FD !

Intrinsic RC limit

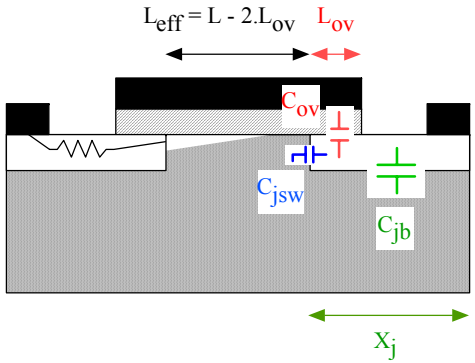
At high frequency, channel = distributed RC line !



⇒ **cut-off frequency = g_m/C_{gs}**

Decreases as L increases !

Extrinsic capacitances



$$C_{L,tot} - C_{L,ext} + C_{jb} \cdot X_j \cdot W + C_{jsw} \cdot 2.(W+X_j)$$

Increases as W increases
⇒GBW decreases !

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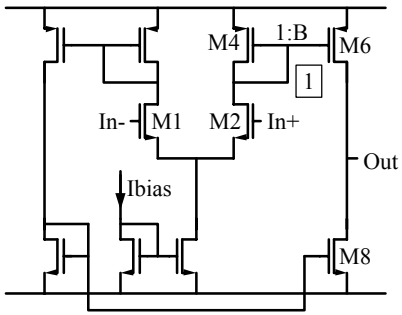
1-stage OTA analysis

GBW model



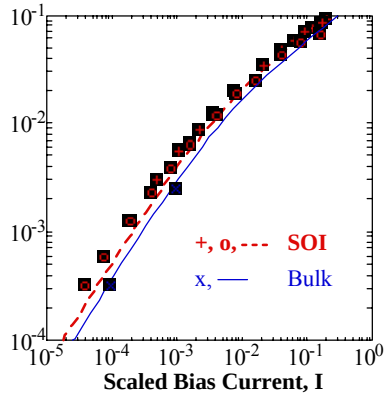
$$f_T = B \cdot \left[\frac{gm}{Id}\right]_{1(2)} \frac{Ibias}{4\check{s}\ C_L}$$

$$A_0 = Vea \left[\frac{gm}{Id}\right]_{1(2)} \qquad Vea = \frac{Vea_6\ Vea_8}{Vea_6 + Vea_8}$$

1-stage OTA

model (lines) vs exp data (symbols)

f_T*C_L/(β*B) Product = (g_m/I_D).I



SOI vs Bulk at constant Ibias ?

↓

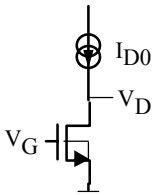
w.i. : n_{bulk} / n_{soi} (36%)

s.i. : (n_{bulk} / n_{soi})$^{-0.5}$ (17%)

Intrinsic stage synthesis

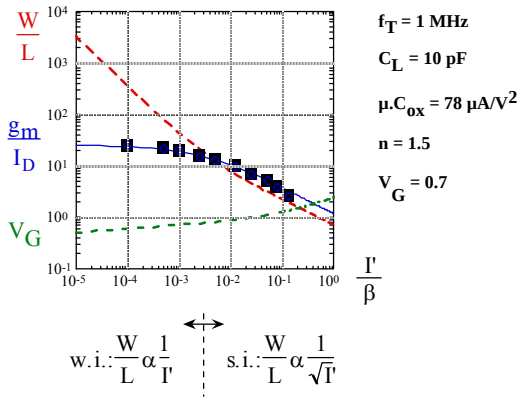
« Gm/Id methodology » based on continuous g_m/I_D vs $I' = I_D/(W/L)$

- Model
- Or experiments



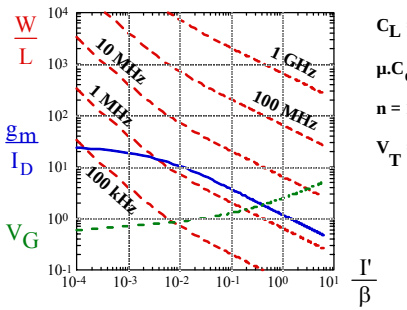
$$g_m = \omega_T . C_L = \left(\frac{g_m}{I_D}\right).\frac{W}{L}.I'$$

$$\frac{W}{L} = \frac{\omega_T . C_L}{\left(\frac{g_m}{I_D}\right).I'}$$

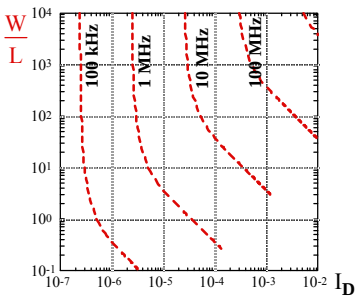


f_T = 1 MHz
C_L = 10 pF
$\mu.C_{ox}$ = 78 µA/V^2
n = 1.5
V_G = 0.7

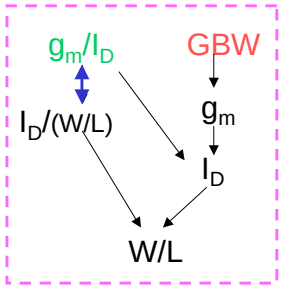
Intrinsic stage synthesis



C_L = 10 pF
$\mu.C_{ox}$ = 85 µA/V^2
n = 1.5
V_T = 0.7



Intrinsic stage synthesis



f_T = 1 MHz
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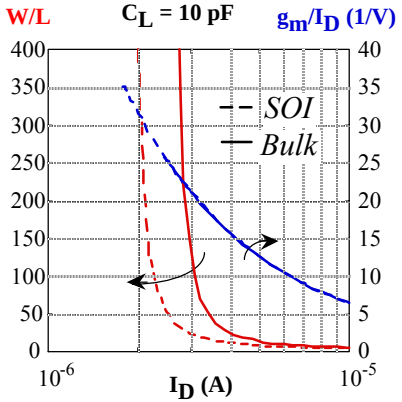
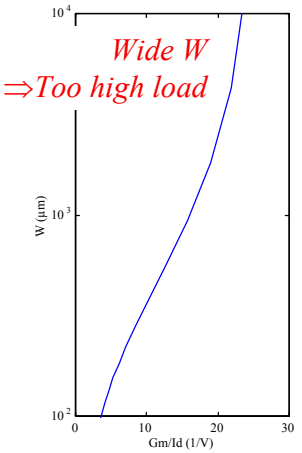
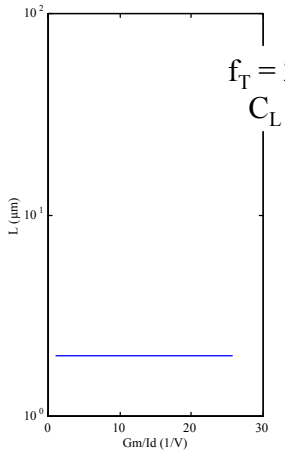


Intrinsic stage synthesis

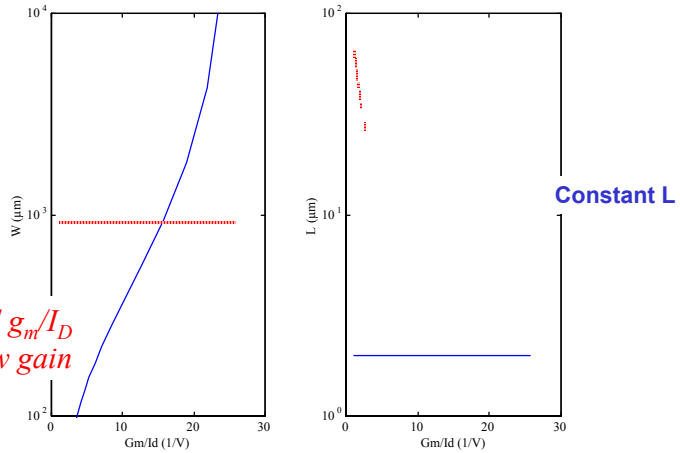
1) Constant L





f_T = 20 MHz
C_L = 10 pF

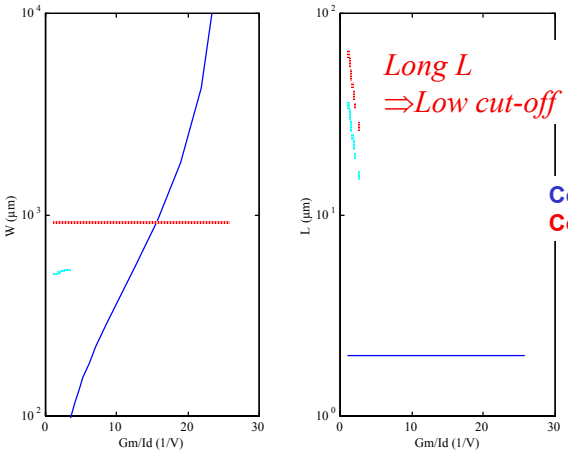
2) Constant W = 0.1 * C_L / (C_{jb}.X_j)



Constant L

Low L and g_m/I_D
⇒Too low gain

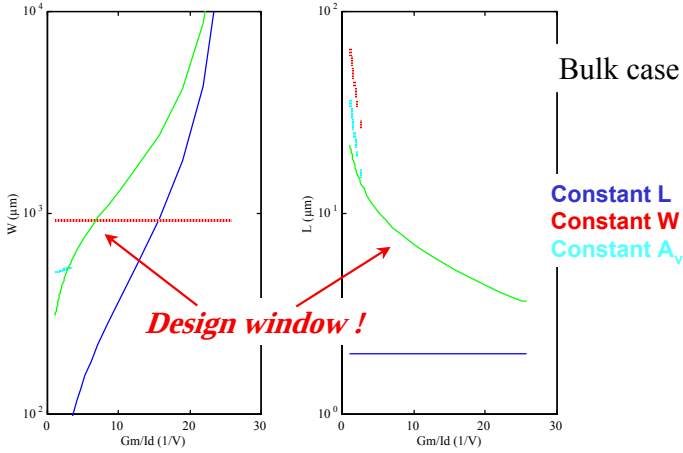
3) Constant A_{v0} = 50 dB



Long L
⇒Low cut-off

Constant L
Constant W

4) Constant cut-off = 2 * f_T *(or C_{gs} = 0.5 * C_L)*



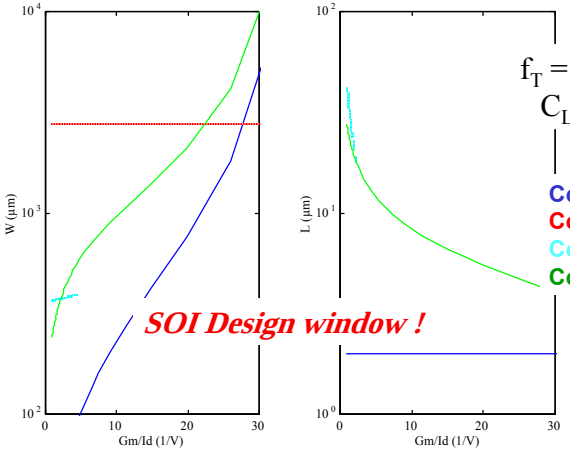
Bulk case

Constant L
Constant W
Constant A_{v0}

Design window !

Intrinsic stage synthesis

SOI case



f_T = 20 MHz
C_L = 10 pF

Constant L
Constant W
Constant A_{v0}
Constant cut-off

SOI Design window !

Example: ‘Demo 1’…

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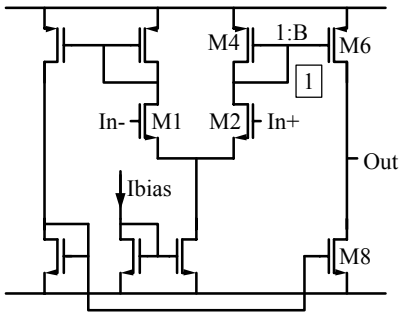
1-stage OTA synthesis

Two-pole model



$$f_T = B \cdot \left[\frac{gm}{Id}\right]_{1(2)} \frac{Ibias}{4\pi C_L}$$

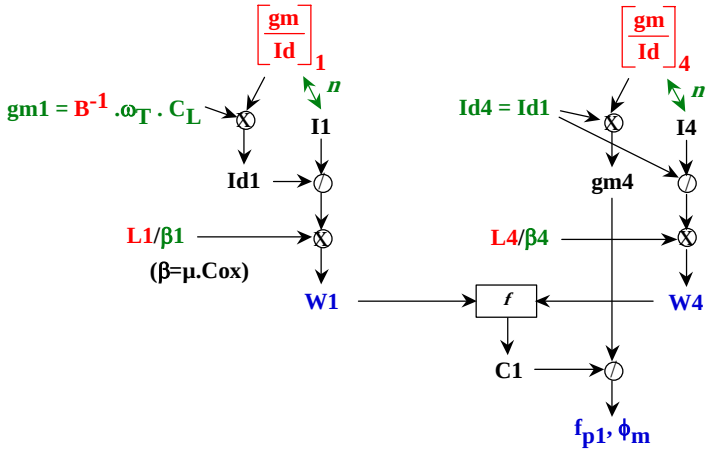
$$A_o = Vea \left[\frac{gm}{Id}\right]_{1(2)} \qquad Vea = \frac{Vea_6\, Vea_8}{Vea_6 + Vea_8}$$

$$f_{p1} = \frac{g_{m4}}{2.\pi.C_1} = \left[\frac{gm}{Id}\right]_4 \frac{I_{d1}}{2.\pi.C_1}$$

$$C_1 = 2/3.C_{ox}.W_4.L_4.(1+B)+C_{jp}.W_4+C_{jn}.W_1 \qquad \phi_m = 90° - \text{atan}\,(f_T / f_{p1})$$

Gm/ID-based synthesis

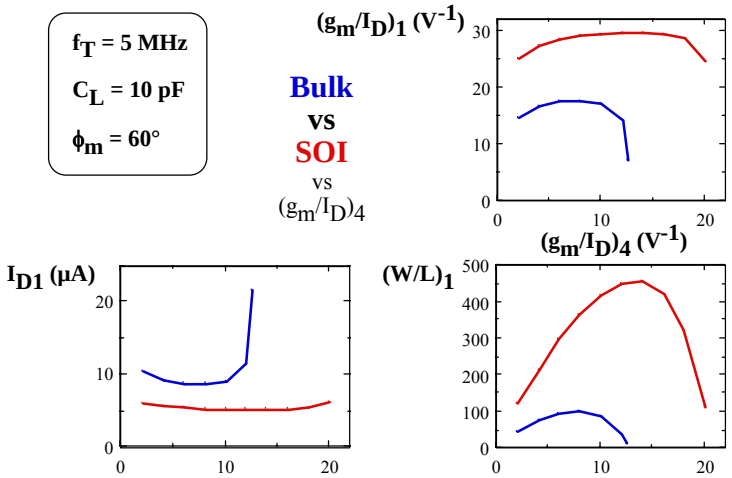
1-stage OTA Design Flow



1-stage OTA synthesis

f_T = 5 MHz
C_L = 10 pF
ϕ_m = 60°

Bulk vs **SOI** vs $(g_m/I_D)_4$



Matching

Current mirror : $\sigma^2\left(\frac{\Delta I_D}{I_D}\right) = \left(\frac{g_m}{I_D}\right)^2 .\sigma^2(V_T) + \frac{\sigma^2(\beta)}{\beta^2}$

$$\sigma^2(V_T) = \frac{A_{V_T}^{\ 2}}{W.L} \qquad A_{V_T} \approx \text{a few mV}.\mu\text{m}$$

(**30** in 2.5 µm Bulk, **13** in 2 µm FD SOI)

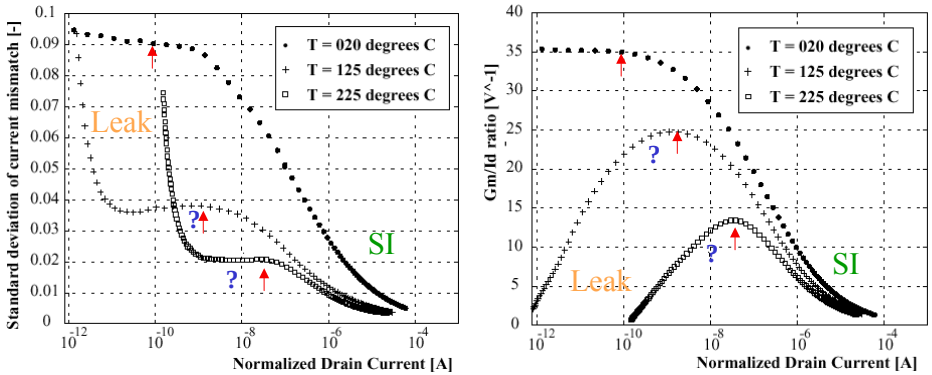
$$\frac{\sigma^2(\beta)}{\beta^2} = \frac{A_\beta^{\ 2}}{W.L} \qquad A_\beta \approx \text{a few \%}.\mu\text{m}$$

(**3** in 2.5 µm Bulk, **5** in 2 µm FD SOI)

SOI vs Bulk: W, L ↗ ⇨ mismatch ↘

Matching

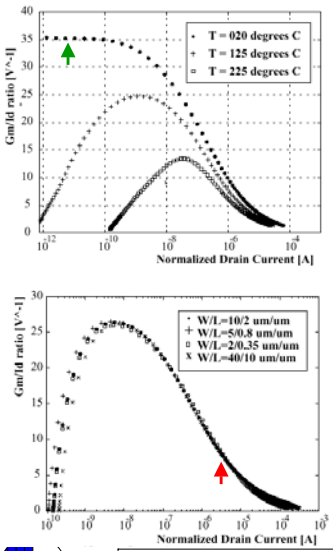
σ((ΔId)/Id) vs Id/(W/L) for SOI FD nMOS
(W/L = 20µm / 10 µm) At different temperatures (Vd = 1.5 V)



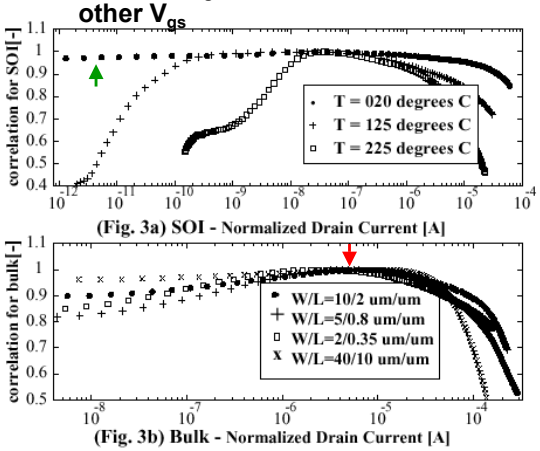
SI: $\frac{\Delta I_d}{I_d} = -\frac{g_m}{I_d}\Delta V_T$ Until Max gm/Id in WI/MI / ??? / Very WI: Leak

WI/MI:

Matching



correlation coefficient between $\Delta I_d/g_m$ at $V_{gs} = V_{th}$ and $\Delta I_d/g_m$ at other V_{gs}



Matching

• In FD SOI, at RT° follows $\frac{\Delta I_d}{I_d} = -\frac{g_m}{I_d}\Delta V_T$ in MI/WI + Δβ in SI

• In bulk/PD
And in FD at HiT°: + another term in MI related to « n (Vgs) »

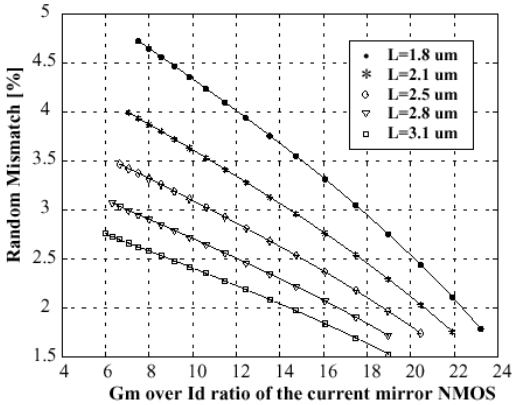
$$\sigma\left(\frac{\Delta I_d}{I_d}\right) = \frac{g_m}{I_d}\sigma(\Delta V_T) + f(v_g)\sigma(\Delta n) + \sigma\left(\frac{\Delta\beta}{\beta}\right)$$

$$\sigma^2(\Delta V_T) = \frac{A_{VTo}^2}{WL};\sigma^2\left(\frac{\Delta\beta}{\beta}\right) = \frac{A_\beta^2}{WL}$$

[Vancaillie, ESSCIRC 2003]

Matching

Design of a current mirror for the input differential pair of an OTA (fixed I_{bias}, fixed $g_{m,mir}/C_{mir} = 4.GBW_{OTA}$)



Improves in MI !
As W.L increases
Faster than gm/Id

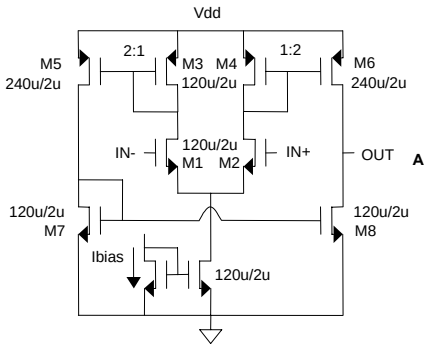
1-stage OTA

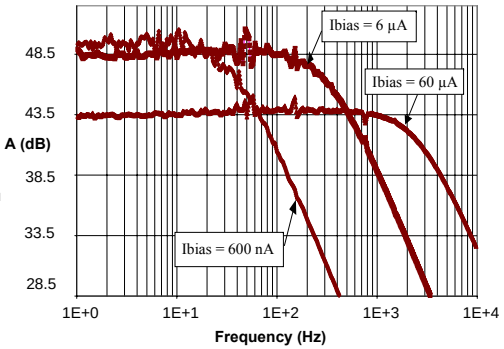
Example

	SOI (design/exp.)	BULK (synthesis)
fT (kHz)	**350**	**350**
Av0 (dB)	**44**	**41**
phase margin (°)	**85.6**	**85.4**
(gm/ID) 1-2	**25.8**	**18**
(gm/ID) 3-6	**22.3**	**14.5**
(gm/ID) 7-8	**22.7**	**14**
(W/L) 1-2	**30/3**	**27/3**
(W/L) 3-4	**33/3**	**23/3**
(W/L) 5-6	**66/3**	**46/3**
(W/L) 7-8	**30/3**	**17/3**
IDD (µA)	**3**	**4.32**
output swing (V) @ Vdd = 1.2 V	**0.9**	**0.75**

1-stage OTA

Micropower experiment on 0.25 µm FD SOI CMOS





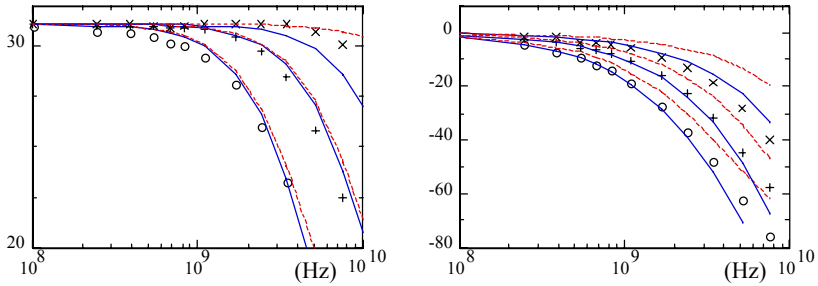
Vdd = 1.5V, g_m/I_D = 15 V^{-1}, $C_L \approx 360$ pF

Example : ‘demo 2’…

1-stage OTA

High-frequency applications

Y_m mag (mS) and phase (°) measurements on 1-µm SOI n-MOSFET

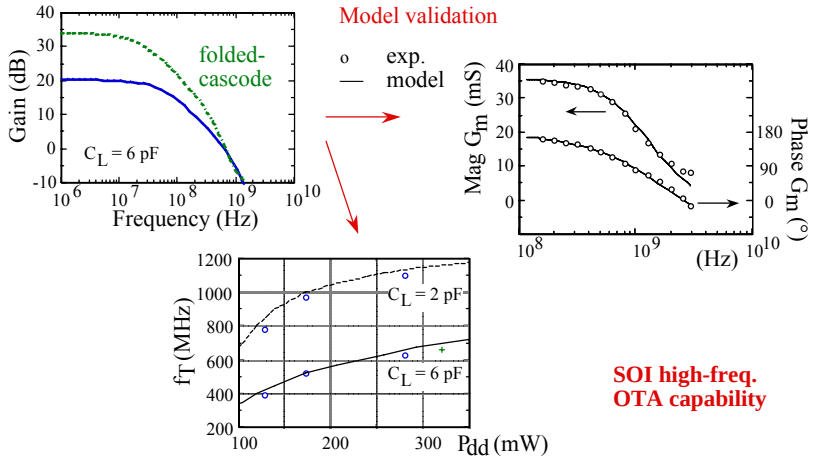


- o 10 * 50/1, Rg = 34Ω/sq.
- \+ 10 * 50/1, Rg = 6Ω/sq.
- × 20 * 25/1, Rg = 6Ω/sq.

- ····· g_{mo} / (1+s.RC)
- —— g_{mo} / (1+s/ω_c) / (1+s.RC)

1-stage OTA

1-stage OTA high-frequency SOI CMOS implementations

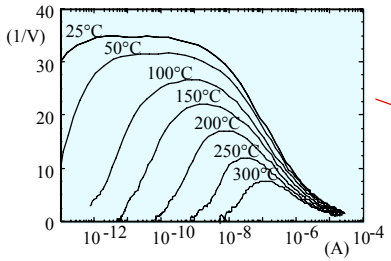


SOI high-freq. OTA capability

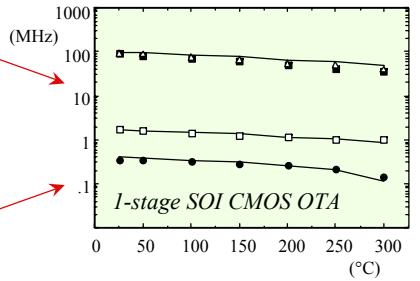
1-stage OTA

High-temperature applications

Gm/Id vs Id/(W/L) vs T



Transition frequency vs T



Mobility vs T

Early voltage vs T → DC open-loop gain vs T

Outline

1/2. Analog Design and Process Assessment with Gm/Id

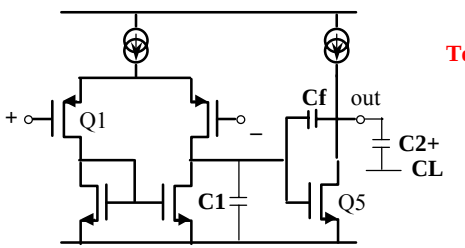
3. Output conductance (Vea), intrinsic capacitances

4. OTA design for low-voltage low-power applications
   - Single-stage micropower OTA
   - Mismatch
   - Applications: high-temperature, high-frequency
   - 2-stage OTAs

\+ Harmonic distortion: filters, mixers
\+ Switches: SC - ADC
\+ Microsystems

2-stage opamp synthesis

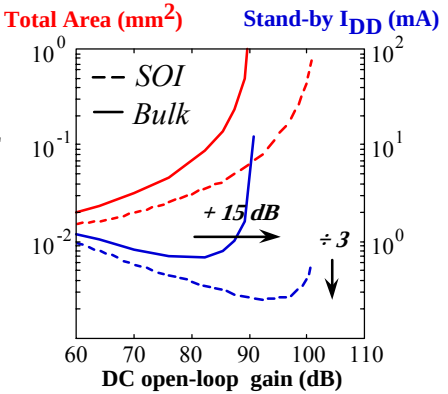
CMOS Miller Op Amp



W/L and C_f ?

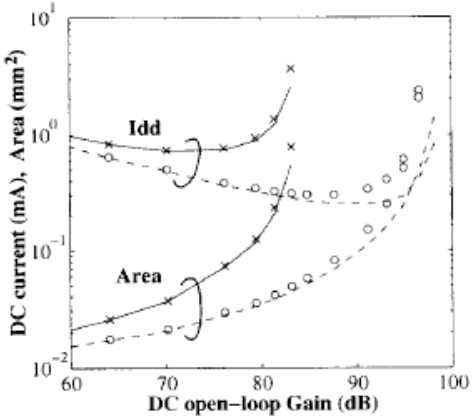
for given f_T, C_L and Φ_m

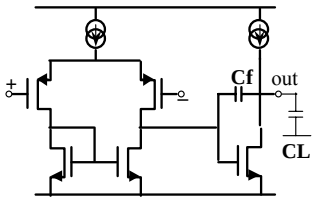
f_T = 10 MHz, C_L = 10 pF, Φ_m = 60°



2-stage opamp synthesis

fT = 10 MHz, CL = 10 pF, Φm = 60°

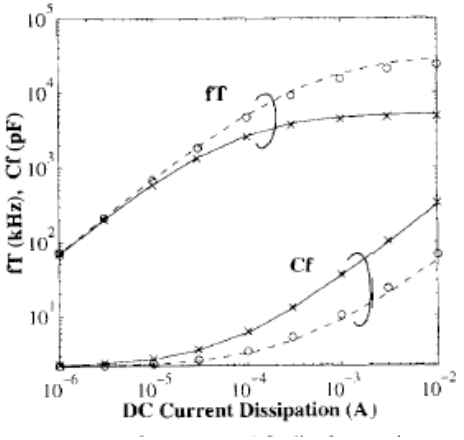




-- o, *SOI*
— x, *Bulk*
o,x **C_{gg5} = 0.76 C_{ox}.W.L**

2-stage opamp synthesis

Avo = 90 dB, CL = 10 pF, ϕm = 60°



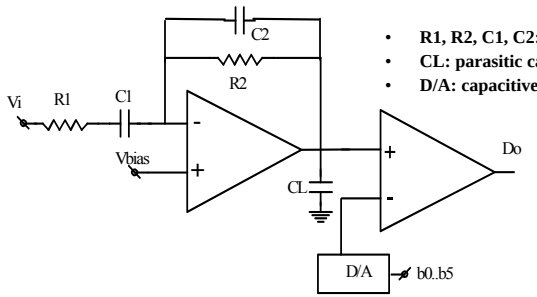
-- o, *SOI*
— x, *Bulk*
o,x **C_{gg5} = 0.76 C_{ox}.W.L**

Same power:
FD => larger fT and SR

OTA applications

Pacemaker Sense Channel

detect spontaneous contraction of the heart chambers



- **R1, R2, C1, C2: external components**
- **CL: parasitic capacitance, specified to 50pF**
- **D/A: capacitive charge redistribution converter**

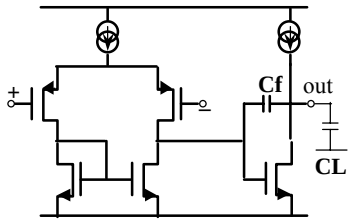
[F. Silveira, D. Flandre, ISCAS 2002]

- **FD SOI Technology**
- **Simpler class AB OTA**
- **and comparator architectures**

⇒ **Record consumption of 110 nA (I.e. one order of magnitude below previous results)**

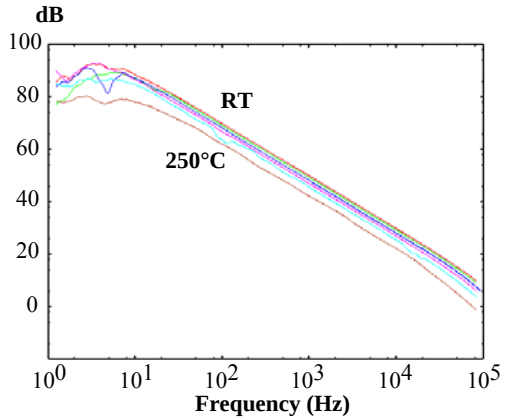
OTA applications

CMOS Miller Op Amp



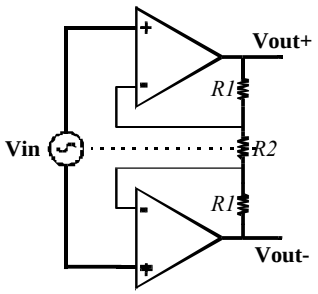
V_{DD} = 3 V

I_{DD} = 3 µA

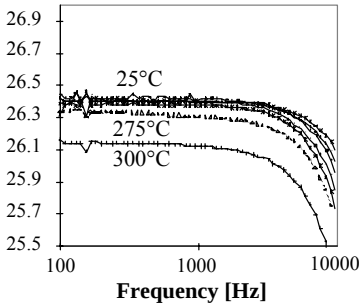


OTA applications

Instrumentation opamp in FD SOI CMOS



Closed Loop Gain [dB]

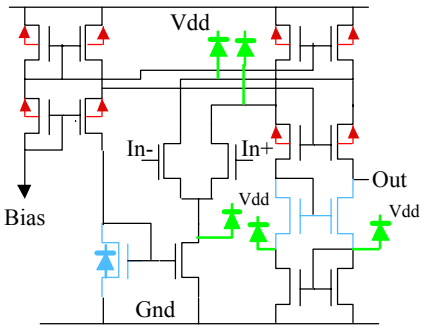


2 Miller OTAs + matched integrated diffusion resistors ⇒ fixed gain of 21 (±0.45%) up to 250°C

High-temp. applications

Design techniques for bulk CMOS analog circuits

Simple folded cascode OTA



Ideas (to balance leakage to substrate) :
- bias circuit : pMOS in separate wells
nMOS sized for same *I*leak as pMOS
- differential pair :
add compensation diodes
- cascode stage : both

but area ↑, consumption ↑, complexity ↑
→ dynamic response ?

In SOI no tricks required

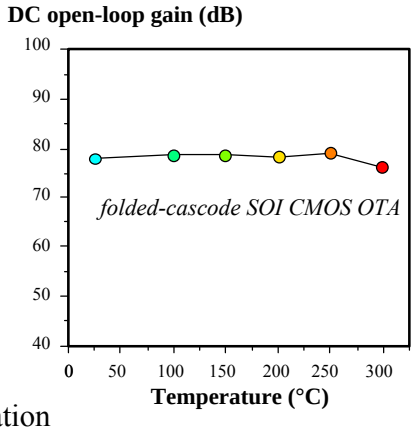
no leakage to substrate
$I_{leak} << I_{saturation}$

Gain - constant
(G_m and G_o↓)

BW ↓ with G_m
(/ 2 at 300°C)

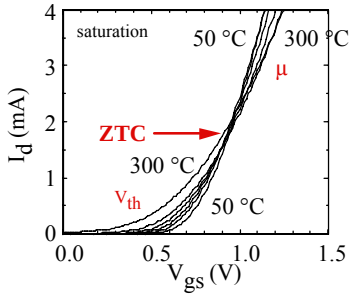
Offset < 2 mV for all T

Constant power dissipation



SOI high-temp design guidelines

- **$(g_m/I_D)_{fT} > (g_m/I_D)_{ndp}$ to preserve stability**
  as higher g_m/I_D degrades more with T
- **optional use of "Zero-Temperature Coefficient point" (ZTC)**



ZTC ° f (V_{ds},V_{bs}, W/L)

SOI : V_{gs} - $V_{th, ZTC}$ - 0.2…0.3 V
bulk : 0.5…1 V