UCL Université catholique de Louvain

General Overview of SOI (Silicon-on-Insulator) technology

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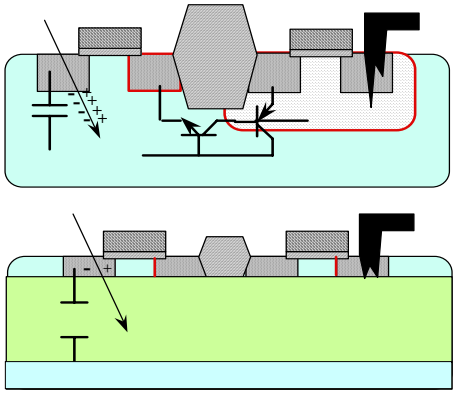
Why Silicon-on-Insulator ?

Bulk CMOS

SOI CMOS



⇒ interesting device and circuit properties with CMOS compatible process !

Outline

1. SOI materials status
2. SOI MOSFETs: types, properties
3. Fully vs Partially-depleted SOI MOSFETs
4. SOI CMOS applications / Roadmap

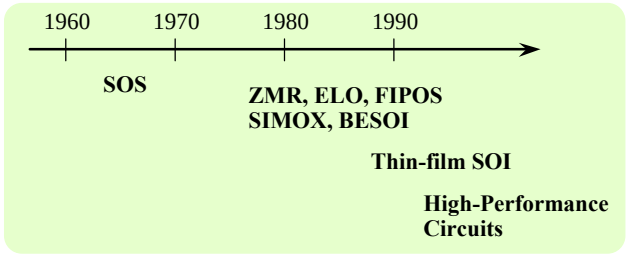
Introduction

Historical Perspective

Year	Field-Effect Devices Si	Field-Effect Devices Others	Others
1930		1st proposal *Lilienfeld/Heil*	
1947			Bipolar *Bell Labs*
1948		thin-film Ge *Shockley*	
1952	JFET - *Shockley*		
1960	MOS - *Kahng/Atalla*		
1961		CdS TFT *Weimer*	
1964	MOS SOS *Mueller*		

SOI

SOI Historical Perspective



Outline of presentation ***1. Evolution of SOI Materials***

2. Characteristics and Models for SOI MOS Devices

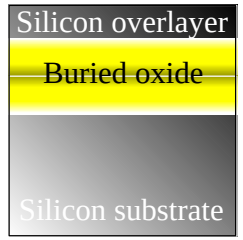
3. Applications of SOI CMOS Circuits

SOI substrates

commercially available SOI substrates

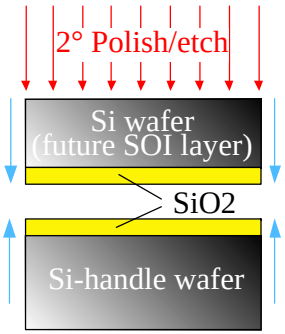
SIMOX

1°Oxygen ion implantation



2° HT annealing

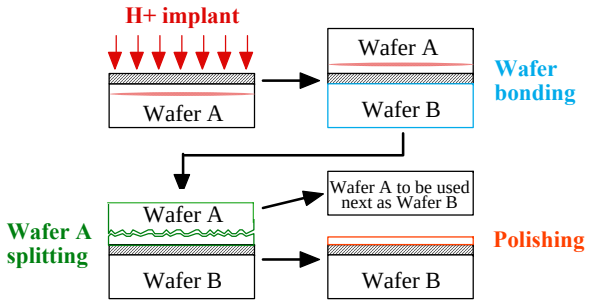
BESOI



1° Bonding

SOI substrates

Smart-Cut® process (LETI)



→ **Unibond wafer (SOITEC)**

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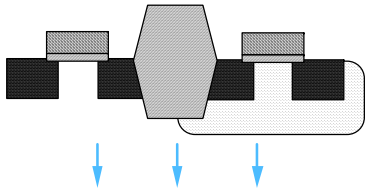
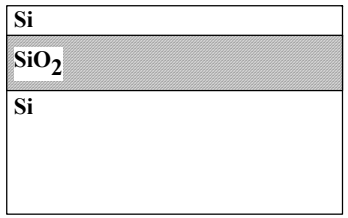
SOI CMOS process

CMOS process



compatible with bulk (same equipment, same steps but optimized

SOI substrate



T_{Si} (0.1-0.5 µm)

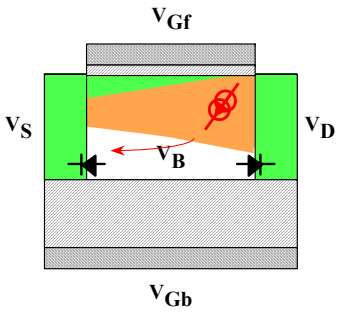
T_{box} (0.3-2 µm)

large choice

if T_{Si} < Field ox. depth
=> no well required !
=> simpler process, no latch-up

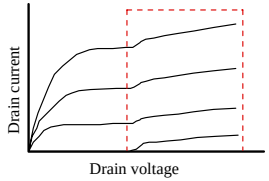
SOI MOSFETs

Partially-depleted MOSFET



Hole current in n-MOS

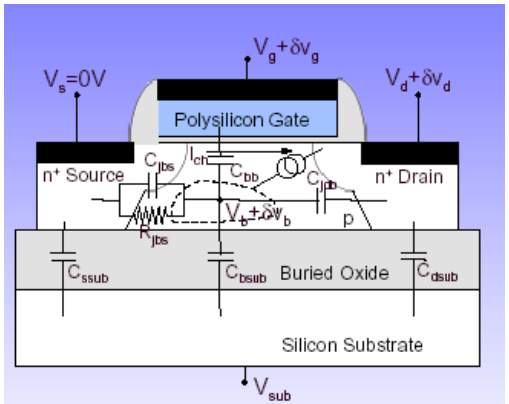
- no V_{Gb}, T_{ob}, Q_{ob}, N_{ob} dependences
- floating substrate node V_B
  - normal operation : $V_B - V_S$
    $V_{ch} - V_B \rightarrow \gamma$ as in bulk
  - far in saturation : I_{ii}
    $V_B > V_S \rightarrow V_{th} \downarrow, I_D \uparrow$
    (kink effect)



Also parasitic bipolar effect !

PD SOI MOSFETs

Dynamic floating-body effects (FBE)



[J. Jomaah, IMEP]

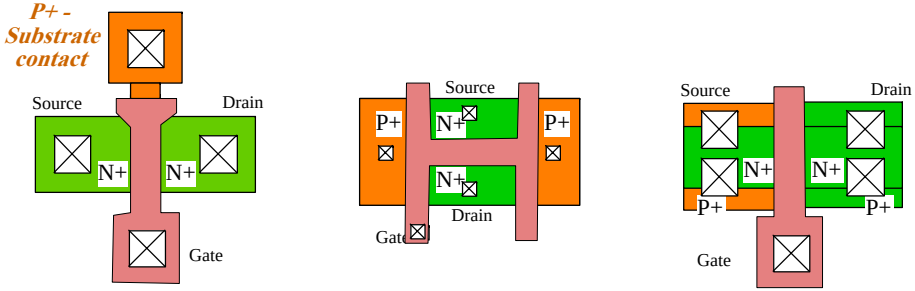
Body coupling to G, S and D =>

• History effects (delays for switch 1, switch 2, steady state… different)

• AC/RF effects on small-signal parameters

SOI MOSFETs

Transistors with body contact

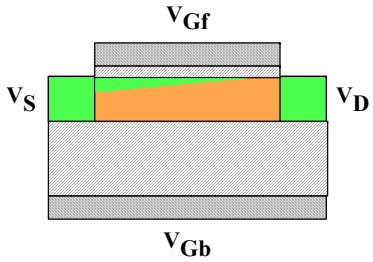


"normal" lateral contact **H-gate contact** Body-tied to S

Trade area vs FBE, but care with tie efficiency !

SOI MOSFETs

Fully-depleted MOSFET



- no clear floating substrate node

  → kink effect almost suppressed !

- V_{Gb}, T_{ob} … dependences of $V_{th,f}$ and I_D

+ reduced body effect
- BOX parameters

Outline

1. SOI materials status

2. SOI MOSFETs: types, properties

3. Bulk vs Fully vs Partially-depleted SOI MOSFETs
   - Body effect
   - Scaling issues

   + Roadmap

4. SOI CMOS applications

SOI CMOS Advantages

Body effect

Saturation current : $I_{Dsat} = \frac{1}{2n} \mu C_{ox} \frac{W}{L} (V_{GS} - V_{TH})^{\alpha}$

Subthreshold swing : $S\,(mV/dec) = n \frac{kT}{q} \ln(10)$

Threshold voltage :

FD: $V_{TH} = V_{fb} + (1+C_d/C_{ox}).2\Phi_f + q.N_a.t_{si}/(2.C_{ox}) - (n-1).(V_{GbS}-V_{Ab})$

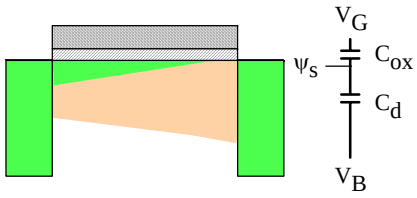
Bulk: $V_{TH} = \ldots + (n-1).V_{bs}$ **where** $n = f(V_{gb})$

PD: Vbs = 0 if FB or body tied to source => V_{TH} constant in a stack !

FD SOI CMOS Advantages

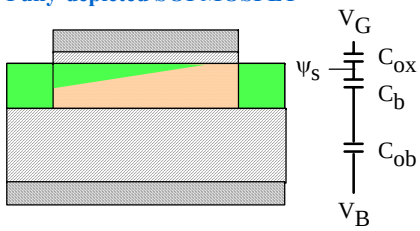
Body effect

Bulk Si MOSFET



$$n = 1 + \frac{C_d}{C_{ox}}$$

Fully-depleted SOI MOSFET



$$n = 1 + \frac{C_b \cdot C_{ob}}{C_{ox} \cdot (C_b + C_{ob})}$$

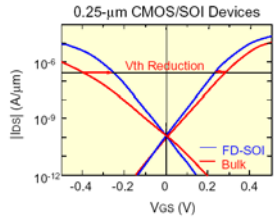
n-body effect factor

	Bulk / FD L = 1.5 µm	Bulk / FD L = 0.25 µm
Tox (nm) Tsi (nm) Tbox (nm)	30 30 80 400	4.5 4.5 30 400
n	1.4 1.1	1.2 1.02

FD SOI CMOS Advantages

Steep Subthreshold Characteristics

Vth Reduction without any Increase in Leakage



NTT Microsystem Integration Labs. T. Douseki

$$Idsat = \frac{1}{2\,n}\,\mu\,Cox\,\frac{W}{L}\,(Vg\text{-}Vth)^{a}$$

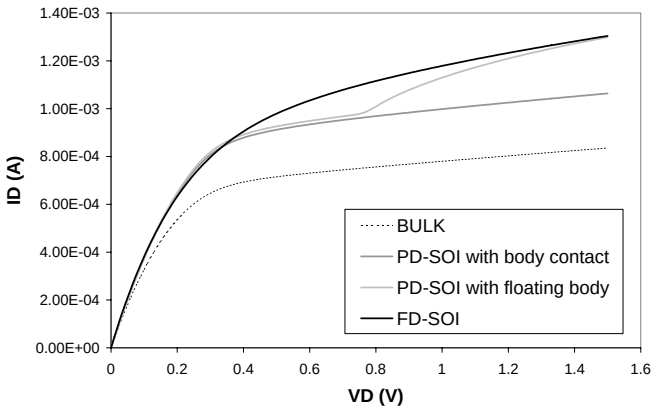
% increase for Vth = 0.5 -> 0.3 V
And Vg = VDD

VDD	a = 1	a = 2
3	1,08	1,17
1,50	1,2	1,44
1	1,4	1,96

Further increase if n reduction taken into account

=> Interest for speed (digital) & dynamic (analog)

Comparison of Bulk, PD and FD SOI MOS Id-Vd



- ♣ BSIM3
- ♦ LETISOI
- ♠ EKV

NMOS

(W=10µ, L=0.25µ)

@ VGS=1V

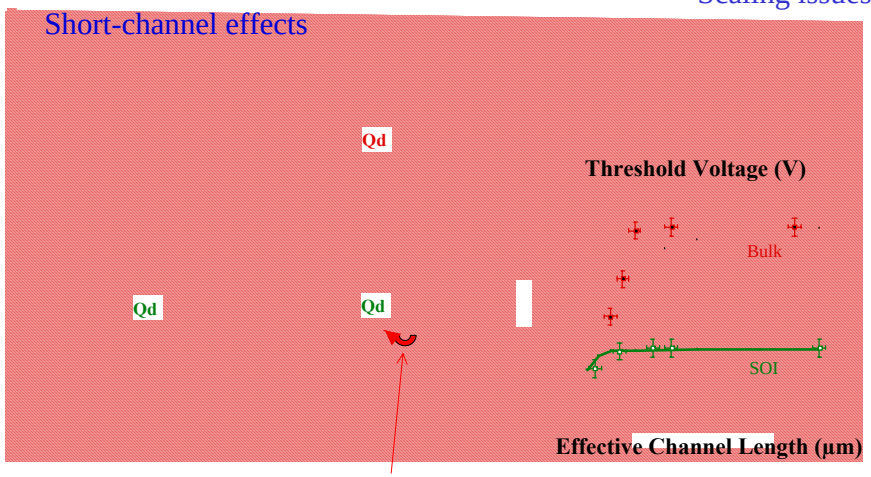
VBS=0V

Scaling issues:

- Short-channel length effects
- Film thickness
- Gate dielectric thickness
- BOX thickness
- Narrow channel, lateral isolation
- Roadmap

Scaling issues

Short-channel effects

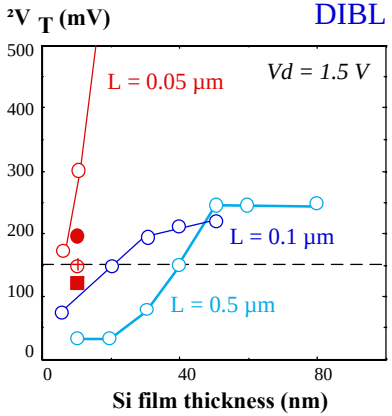


But: 2D back interface problem below 0.2 µm !

Scaling issues

Deep submicron simulations

DIBL = Vth dependence on Vd



○ $Na = 5.10^{17}\ cm^{-3}$, $t_{ox} = 4.5\ nm$
● $3\ nm$
⊕ $2\ nm$

■ $Na = 1.10^{15}\ cm^{-3}$, $t_{ox} = 3\ nm$

[E. Rauly, INPG, 1999]

Scale Tsi, Tox, Tbox !

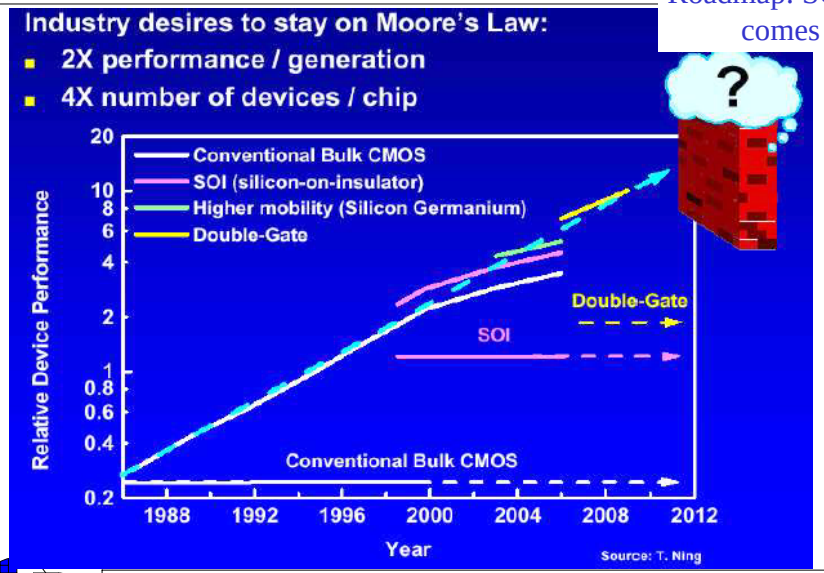
Roadmap

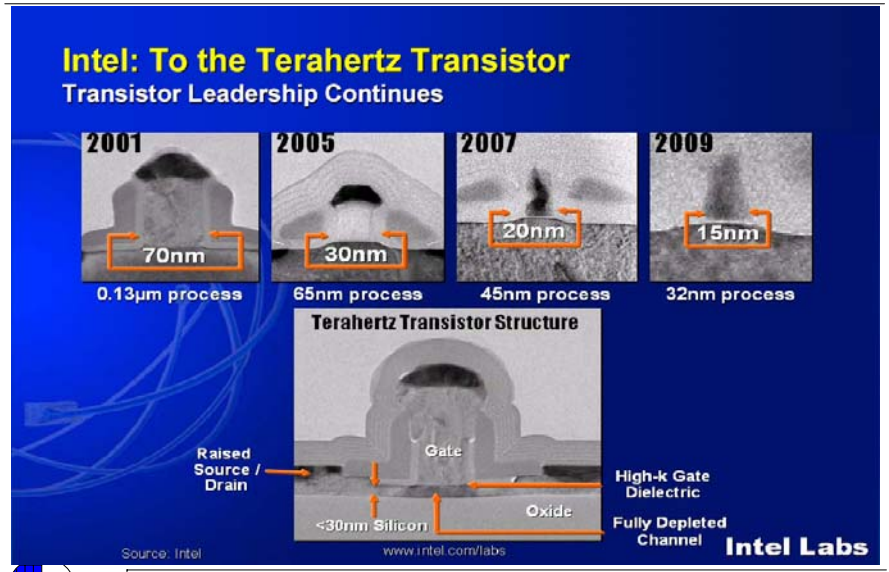
Present SOI CMOS process status:

- **Industrial preference for PD (IBM, AMD, STM…):**
  - **less dependence than FD on SOI wafer « precision »**
  - **almost direct transfer of bulk CMOS**
  - **known scalability below 100 nm**

- **with a few important exceptions:**
  - **for FD present known advantages (OKI, NTT… 0.15 µm)**
  - **for niche applications (Marin, Peregrine… 0.5 µm)**
  - **for future (ITRS < 65 nm, Intel !!!)**

Roadmap: SOI comes in





Outline

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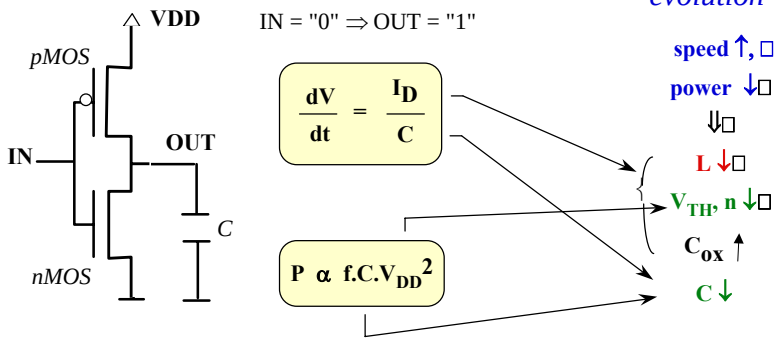
   - digital: LVLP
   - special: high-temperature

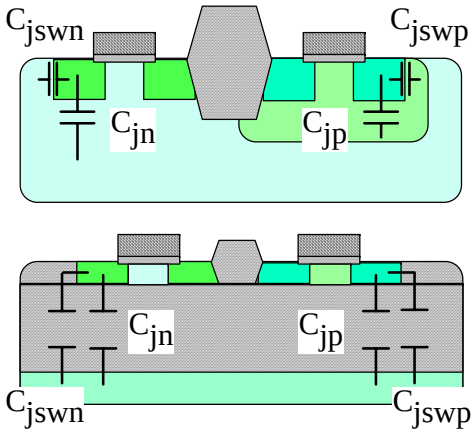
LPLV

CMOS Inverter



LPLV

Parasitic Capacitances



Bulk CMOS

C_{jn} - 0.18 / C_{jp} - 0.4 fF/µm²

C_{jswn} - 0.4 / C_{jswp} - 0.5 fF/µm

SOI CMOS

C_{jn} - 0.06 / C_{jp} - 0.06 fF/µm²

C_{jswn} - 0.05 / C_{jswp} - 0.05 fF/µm

C_{poly} bulk / SOI - 1.5

C_{metal1} bulk / SOI - 1.3

Junction capacitance in 0.25 µm CMOS:

		BULK	PD-SOI	FD-SOI
Cj	NMOS	7.28e-4 F/m^2	5.2e-5 F/m^2	5.2e-5 F/m^2
	PMOS	6.15e-4 F/m^2	8.5e-5 F/m^2	8.5e-5 F/m^2

Effect on 16-bit 1.5V-adder in 0.25 µm Bulk and FD:

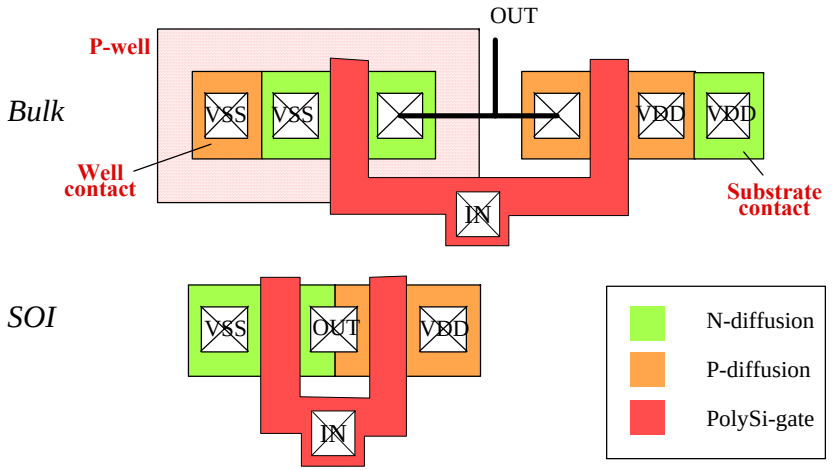
Delay

Div.	Bulk	Mult.	FD-SOI
10	1.542 ns	**1**	1.467 ns
1	1.833 ns	**10**	2.218 ns

Dynamic Power

Div.	Bulk	Mult.	FD-SOI
10	8.396 mW	**1**	6.347 mW
1	9.654 mW	**10**	8.843 mW

Layout of CMOS inverter



general agreement : ↓ $C_{parasitic}$ ⇒ ↑ Speed by 30…40%

+

predictions : ↓ V_T and *n* ⇒ add ↑ by 30…60% at Vdd = 2…3 V

realistic ?

CMOS Gate Arrays(Mitsubishi,IEDM) ⟶ SOI vs Bulk

1991	**16k**	**0.6 µm**	**FD (unoptimized)**	**ring osc.** **16x16b mult.**	**1.4 x speed, Vdd = 3** **0.7 x power**
1993	**1M**	**0.5 µm**	**FD (optimized)**	**"**	**1.7 x speed, Vdd = 3** **0.7 x power** **2.0 x speed, Vdd = 2** **0.5 x power**

Product announcements:

- **IBM: since 1998, mainframe processors, Power PC … on SOI (PD, now below 100 nm)**
- **Motorola: 1 Million Apple G4 shipped in 2002 (PD)**
- **AMD: high-end microprocessor on SOI in 2003 (PD)**

- **High-temperature niche: Honeywell, XFAB (PD)**

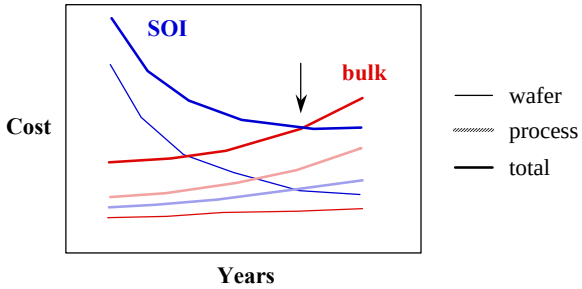
- **Micropower niche:**
  - **watches: Seiko (PD), Swatch (FD)**
  - **« Green energy »: NTT (FD)**

- **RF components:**
  - **Peregrine (FD)**
  - **Silicon wave: Bluetooth (BiCMOS)**

Perspectives

Competitiviness

[Colinge]



[Sematech] **+ higher performances → higher selling price**

⇓

256 kb SRAM SOI cheaper even if wafer = 2…3 x bulk !

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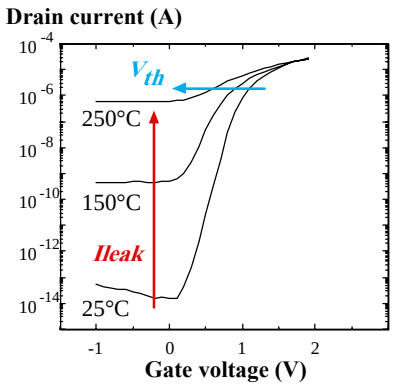
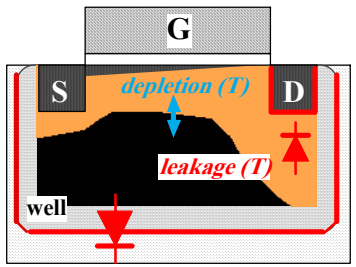
High-temperature

Physical origin of leakage



$V_{th} \propto X_{dmax}$

Bulk Si MOSFET



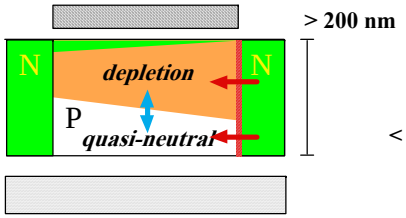
$I_{leak} \propto A_j \cdot n_i$ (gen) up to 150°C

n_i^2 (diffusion) above

High-temperature

SOI (Silicon-on-Insulator)

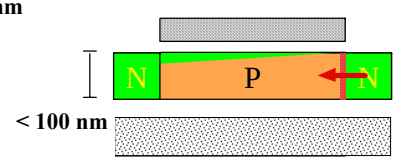
Partially depleted (***PD***)



$I_{leak} \propto W.T_{si} \cdot n_i^2$ (diffusion)

$$\frac{\check{Z}V_{th}}{\check{Z}T} = \frac{\check{Z}\Phi_f}{\check{Z}T} + k \cdot \frac{\check{Z}X_d}{\check{Z}T}$$

Fully depleted (***FD***)

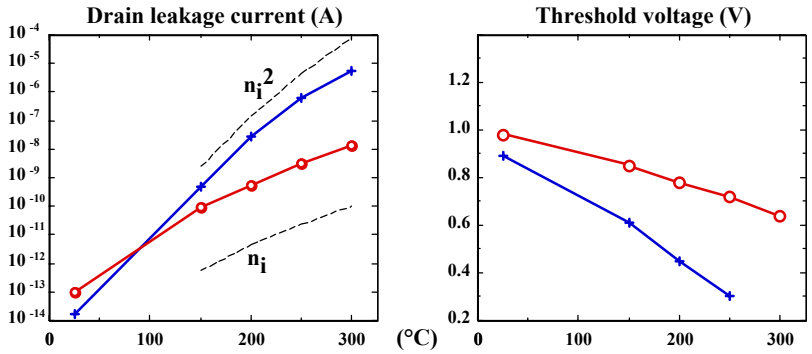


$I_{leak} \propto W.L.T_{si} \cdot n_i$ (generation)

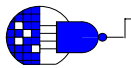
$\check{Z}V_{th} / \check{Z}T = (1+\varepsilon) \cdot \check{Z}\Phi_f / \check{Z}T$

High-temperature

bulk vs FD SOI MOSFET

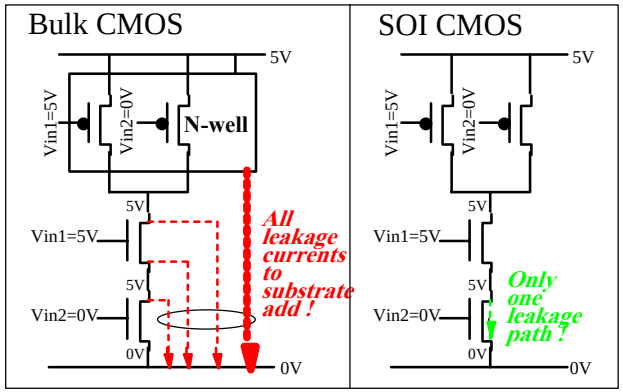


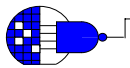
bulk: 1 µA / µm width at 300°C — 2…4 mV/K
FD SOI: 1 nA / µm " " — 0.7…1.5 mV/K



High-temperature

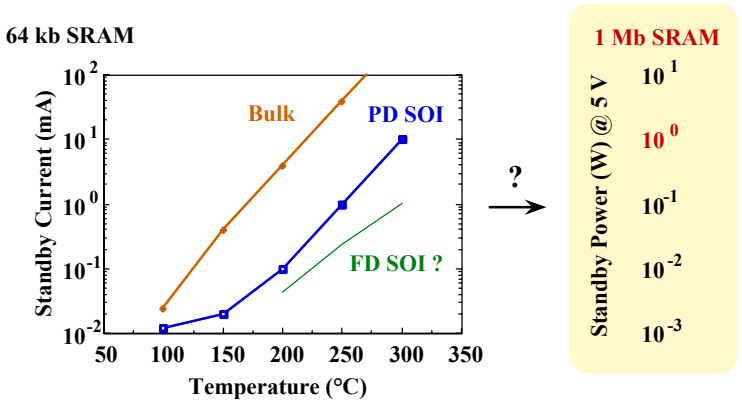
Current Leakage



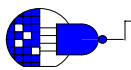


High-temperature

- I_{leak} ?



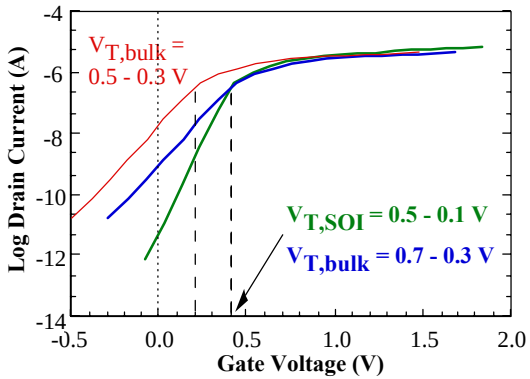
[Honeywell, 3rd High Temperature Electronics Conf., June 96, p.XI-3]

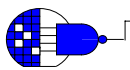


Perspectives

What about static leakage ?

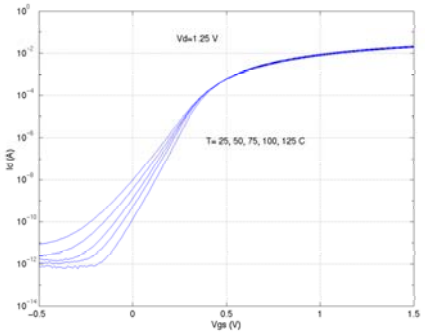
Extrapolation of Device Characteristics at 400K





Perspectives

I_d vs. V_{gs} at different temperatures and V_d=1.25 V for
FD SOI nMOSFET with L=0.35 µm (L_{eff}=0.26 µm) and W=105.6 µm.

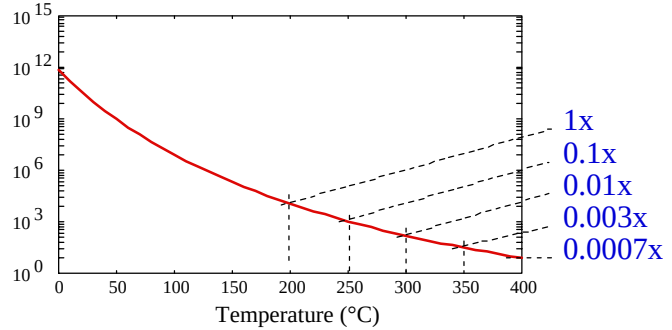


for 100°C and L = 0.35 µm, I_{off} ≈ 30 pA/µm for SOI vs 400 pA/µm in bulk !

Perspectives

Burn-in Test and IDDQ testing implications !

Time to failure (arb. units)



⇒ higher functional temperature ⇒ lower test cost !