# Very Low Voltage Analog Circuit Design

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# Motivations for LV Design

- Historically: Battery operated systems (ex. Wrist Watch) -> 3V , 1.5V
- Mobile equipments
- Reduction of Supply Voltages of VLSI Technologies for Mixed-Signal Devices:
  5V -> 3V -> 2.5V -> 1.8V
- Ultimate Supply Voltage: 1V for .1µ CMOS
  -> Ultra Low Voltage Design



# Problems of LV design

- Reduction of $V_{DD}$ faster than $V_T$

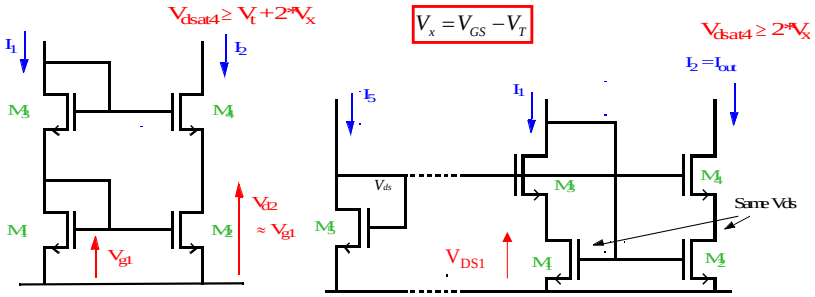
| Technology | $V_{DD}$ | $V_T$ |
|---|---|---|
| .8 µ | 5 V | 750 mV |
| .35 µ | 3.3 V | 550 mV |
| .25 µ | 2.5 V | 450 mV |
| .18 µ | 1.8 V | 400 mV |
| .12 µ | 1.2 V | 350 mV |



# Problems of LV design (cont.)

- Reduced headroom for biasing
  -> ex: cascode transistors
- Signal swing reduces faster than supply voltage
  -> increase in power consumption
  -> increase in area (larger capacitors)
- Some circuits are no longer functional:
  -> voltage switch

# LV cascode current mirror




Cascode Current Mirror

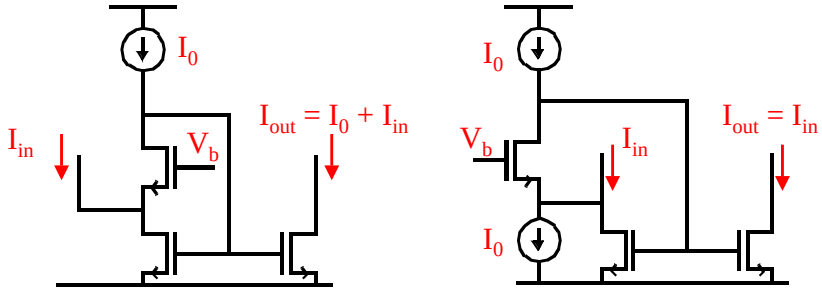
Low Voltage Cascode Current Mirror

$(V_{gs5} - V_t) \geq 2 \cdot (V_{gs1} - V_t)$

$I_5 = I_1 \Rightarrow K_5 \leq \frac{K_1}{4}$



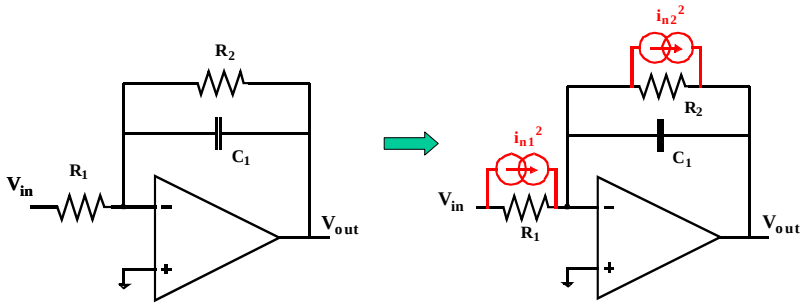
# Ultra-low-voltage current mirror




Very low minimum input + output voltages ( > $V_x$ )



# SNR

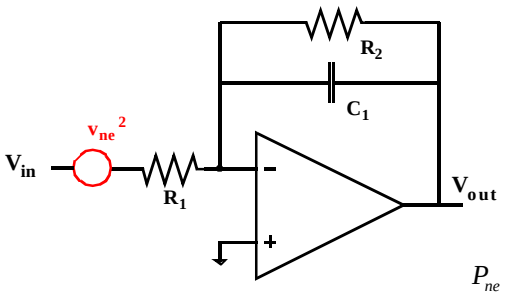



$$P_{S_{in}} = \frac{v_{in}^2}{2} \leq \frac{(V_{DD} - V_{SS})^2}{4}$$

$$S_{In_1} = \frac{4kT}{R_1} \qquad S_{In_2} = \frac{4kT}{R_2}$$



# SNR vs. $V_{DD}$




$$S_{Vne} = 4kT \cdot (R_1 + R_2)$$

$$f_{bn} = \frac{\pi}{2} f_b = \frac{\pi}{2} \cdot \frac{1}{2\pi R_2 C_1}$$

$$P_{ne} = \frac{4kT \cdot (R_1 + R_2)}{4 R_2 C_1} = \frac{kT}{C_1} \cdot \left(1 + \frac{R_1}{R_2}\right)$$

$$SNR_{\max} = \frac{P_{Sin_{\max}}}{P_{ne}} = \frac{(V_{DD} - V_{SS})^2}{4} \cdot \frac{C_1}{kT} \cdot \frac{R_2}{R_1 + R_2} \propto (V_{DD} - V_{SS})^2 \cdot C_1$$

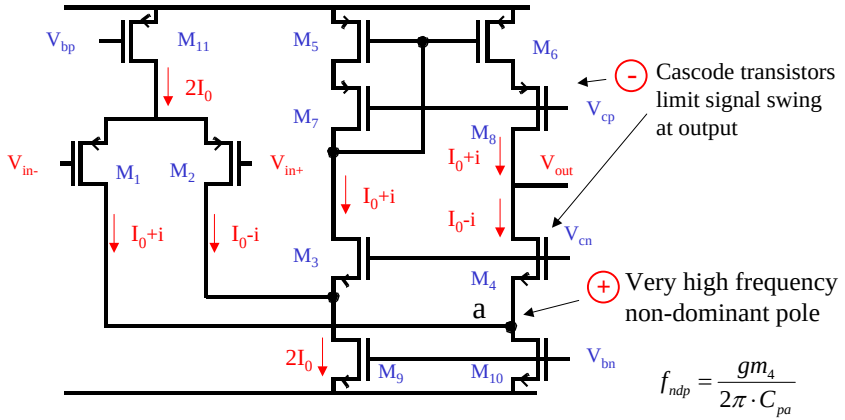
# Consequences of $V_{DD}$ reduction

- Power remains constant (in first approximation)
  $V_{DD}$ decreases -> $I_{DD}$ increases
- Area increases with the inverse of the square of the supply voltage at constant SNR

$$Area \propto C_1 \propto \frac{SNR}{(V_{DD} - V_{SS})^2}$$

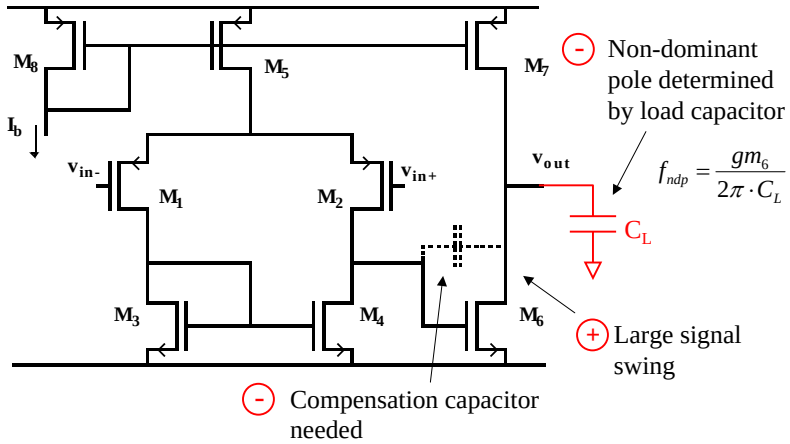


# Ex.: Folded Cascode OTA



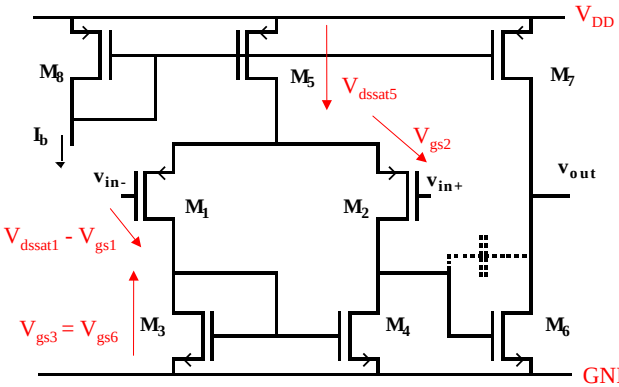



# Preferred: 2-stage amplifier






# Input common mode limitation



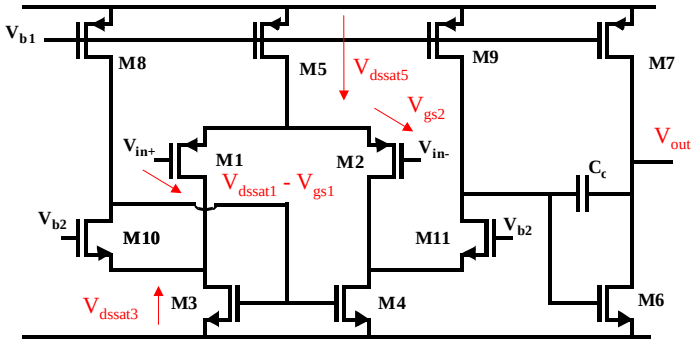

$v_{in+} - v_{in-} <<$

$V_{CM_{MIN}} = V_{GS_3} + V_{GS1} - V_{DSSAT_1} = V_{GS_3} + V_{TP}$

$V_{CM_{MAX}} = V_{DD} + V_{DSSAT_5} + V_{GS_2}$

$\Rightarrow \quad V_{DD_{MIN}} = V_{GS_3} - V_{DSSAT_1} - V_{DSSAT_5}$

# Ultra-LV OPAmp




$$V_{CM_{MIN}} = V_{DSSAT_3} + V_{TP} \le 0$$

$$V_{CM_{MAX}} = V_{DD} + V_{DSSAT_5} + V_{GS_2}$$

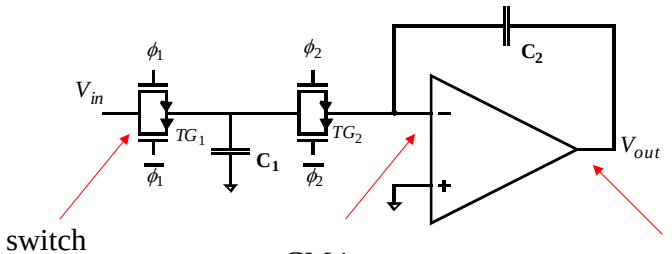
$$\Rightarrow \quad V_{DD_{MIN}} = -V_{DSSAT_5} - V_{GS_1}$$

$$V_{CM} = 0$$



# Constraints for ULV Design

- Typical SC integrator



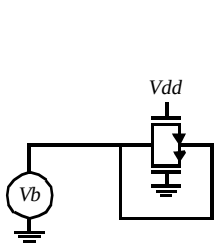

switch conductance

CM input voltage range

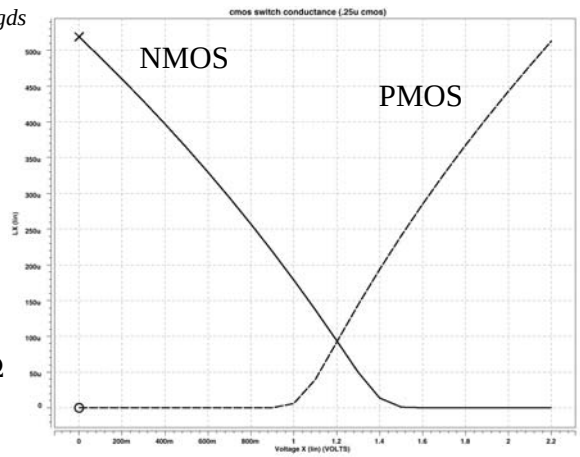
output voltage range



# Switch conductance at 2.2V



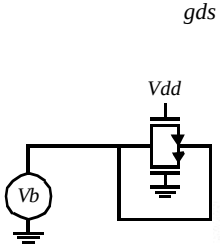

gds



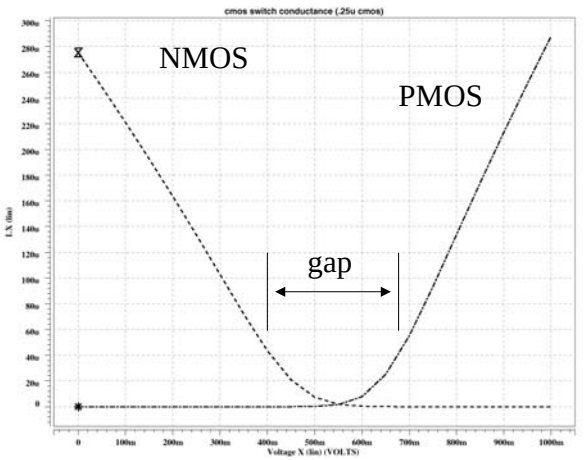

Rswitch < 5kΩ



# Switch conductance at 1V




gds



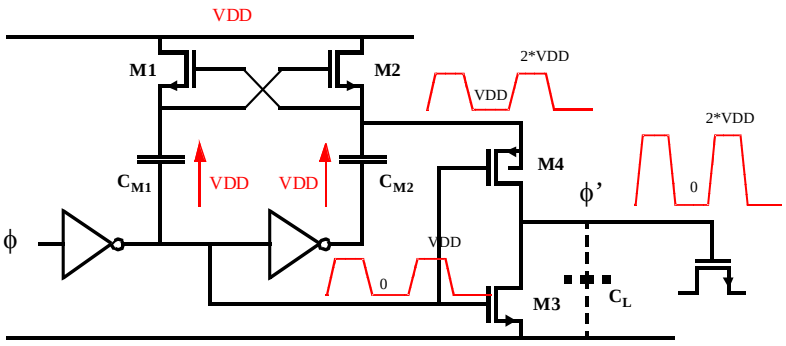

Rswitch # 1MΩ

# Solution Strategies

- DC-DC converter
  increase supply voltage of analog circuit
- Clock-voltage multiplication
  increase driving voltage of switches
- Switched Opamp
- Clock-voltage bootstrap
  controlled increase of switch driving voltage



# Clock voltage multiplication




$Q_{pump} = (2V_{DD}-V_{outH})*C_{M2}$

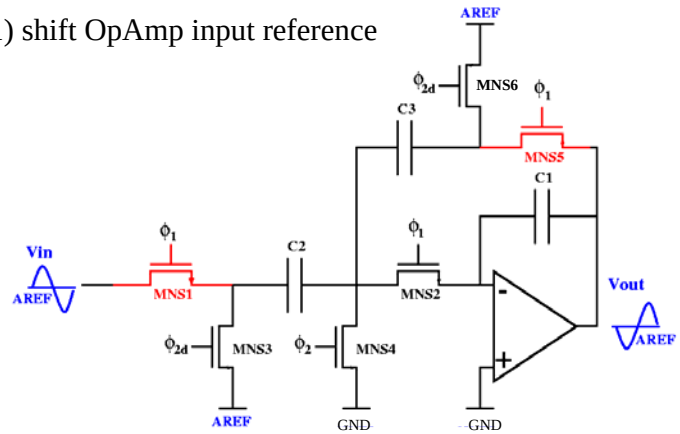
$Q_{CL} = V_{outH}*C_L$

$$V_{outH} = 2 * V_{DD} * \frac{C_{M2}}{C_{M2}+ C_L}$$



# Principle of Level Shifting (1)

1) shift OpAmp input reference

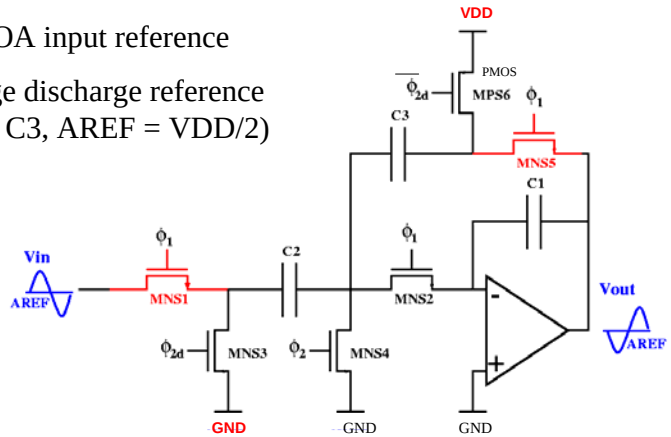




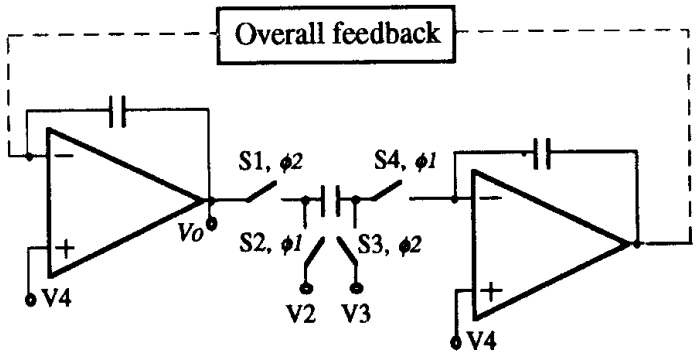

# Principle of Level Shifting (2)

1) shift OA input reference

2) change discharge reference
(C2 = C3, AREF = VDD/2)



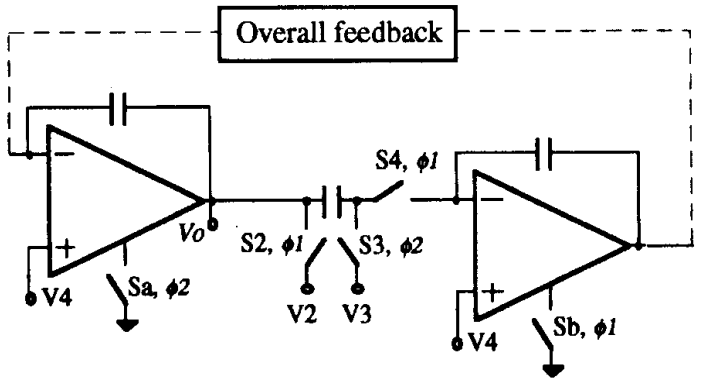
# Conventional SC integrator




(a)



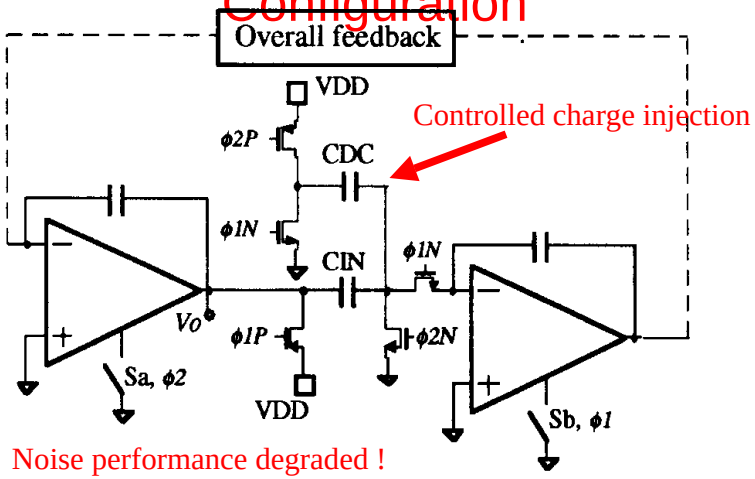
# Switched Opamp SC Integrator




Pb: multiple reference voltages!



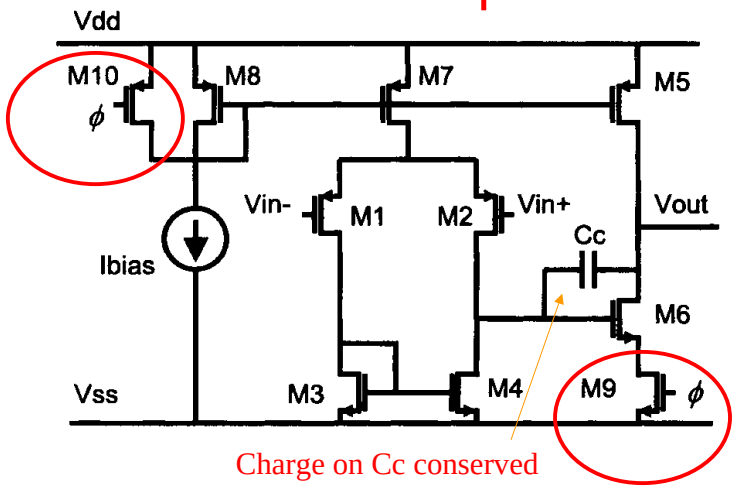
# Improved Integrator Configuration




Noise performance degraded !



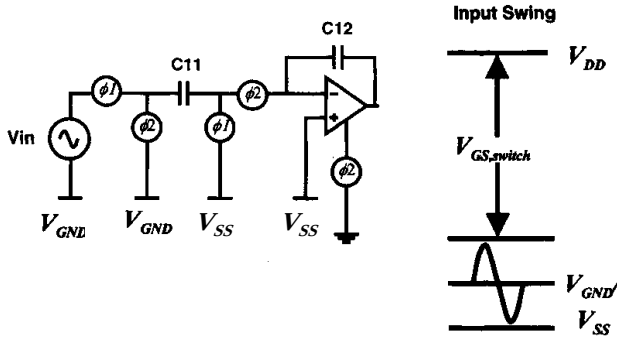
# Switched Amplifier




Charge on Cc conserved

Peluso, Steyaert, KUL, Leuven

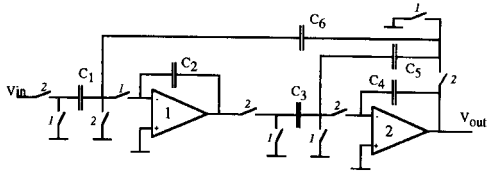
# Input switch configuration



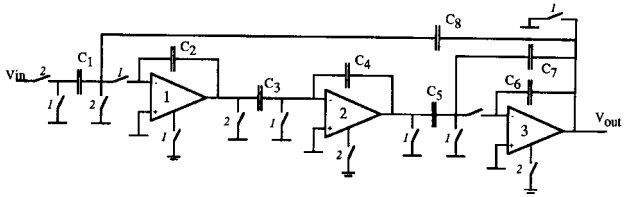

Major limitation: input swing!



# Biquad Filter Structure



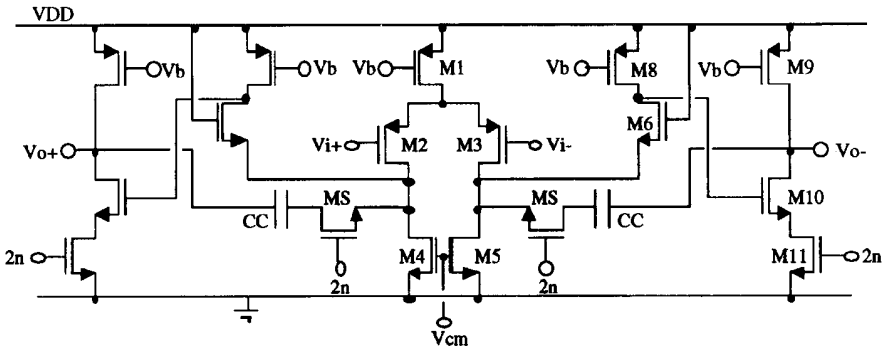

(a) Conventional




(b) Switched Opamp



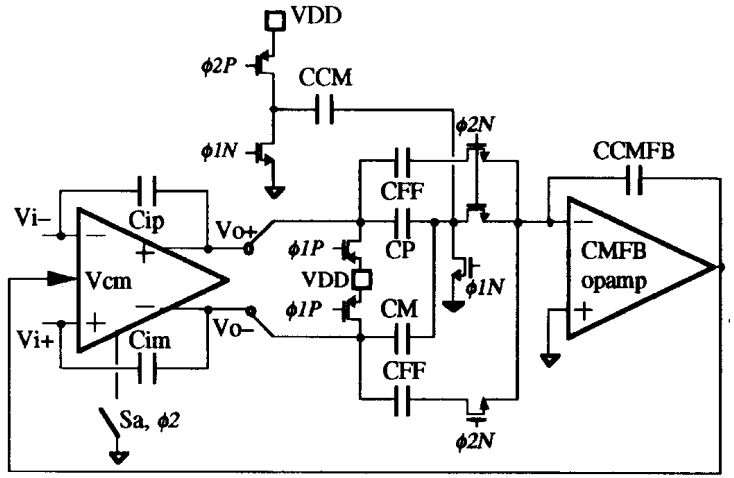
# LV Differential Amplifier



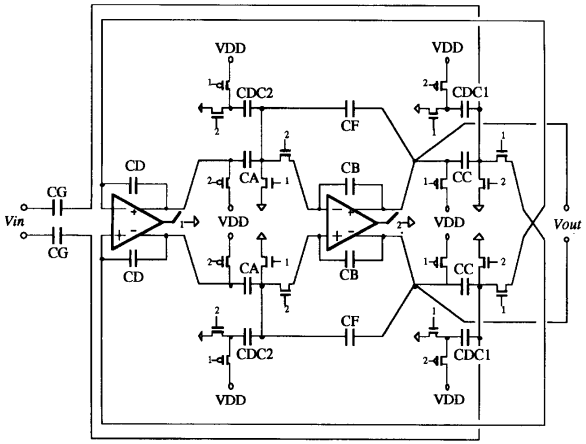

2-stage structure
Cascode transistors for level shifting
No switching of bias voltage



# Differential Config: CMFB



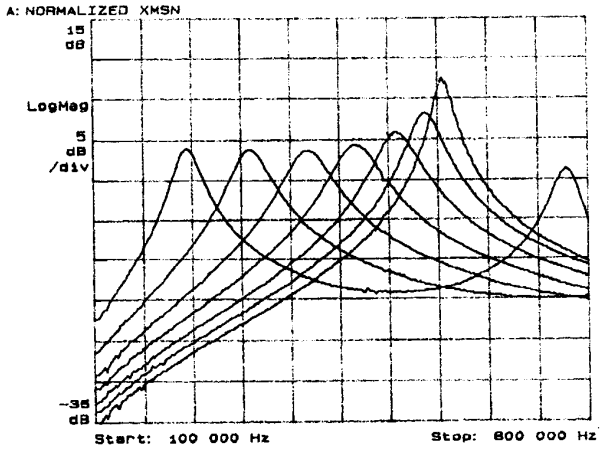
# Design Example: Bandpass filter




Baschirotto, Castello, Univ. Pavia



# Band-pass Filter: Results (1)





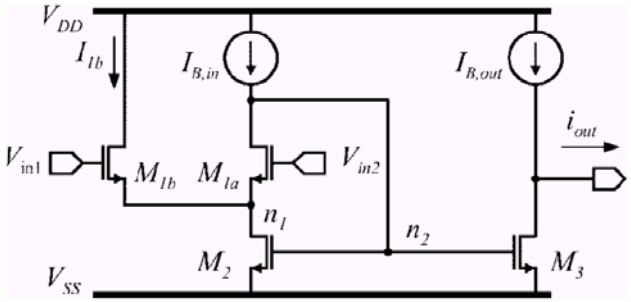

# Band-pass Filter: Results (2)

TABLE III
FILTER PERFORMANCE

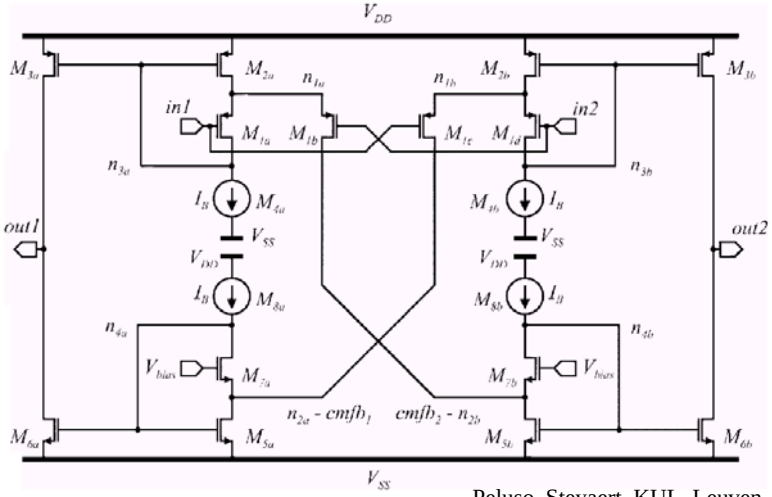
| | |
|---|---|
| Technology | 0.5-$\mu$m CMOS |
| Supply voltage | 1 V |
| Power consumption | 160 $\mu$W |
| Sampling frequency | 1.8 MHz |
| Q | 6.6 |
| fo | 435 kHz |
| Max. output swing | 1.6 Vpp |
| Total output noise | 800 $\mu$Vrms |
| THD 1% | 725 mVpp |
| THD 3% | 1.1 Vpp |
| IM3 1% | 800 mVpp |
| IM3 3% | 1 Vpp |
| Dynamic range (IM3 3%) | 52 dB |
| PSRR | -46 dB |
| Filter chip area | 0.15 mm$^2$ |



# ULV Differential Amplifier



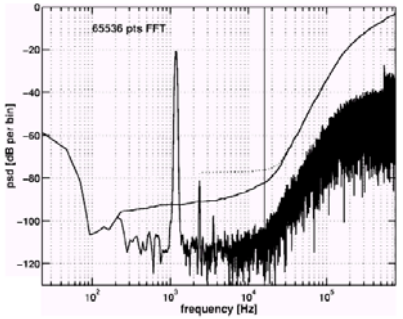
# ULV Class A-B Amplifier




Peluso, Steyaert, KUL, Leuven



# 1V Δ–Σ Converter



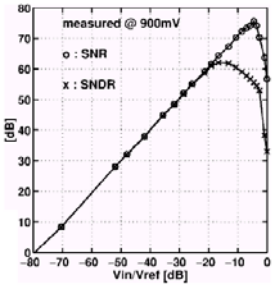



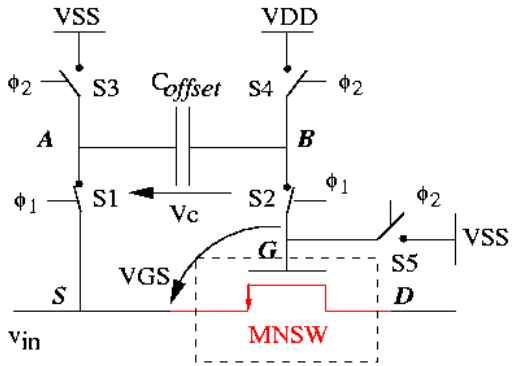

TABLE III
PERFORMANCE SUMMARY OF 900-mV ΔΣ MODULATOR

| | | |
|---|---|---|
| Signal Bandwidth | 200-16000 | *Hz* |
| Sampling Frequency | 1.538 | *MHz* |
| max. diff. input level | 500 | $mV_{pp}$ |
| *DR* | 77 | *dB* |
| peak *SNR* | 76 | *dB* |
| peak *SNDR* | 62 | *dB* |
| Supply voltage | 900 | *mV* |
| Power consumption | 40 | $\mu W$ |
| chip core area | ca. 0.85 | $mm^2$ |
| Techology | 0.5 | $\mu m$ std. CMOS |

Peluso, Steyaert, KUL, Leuven



# Clock Voltage Bootstrap

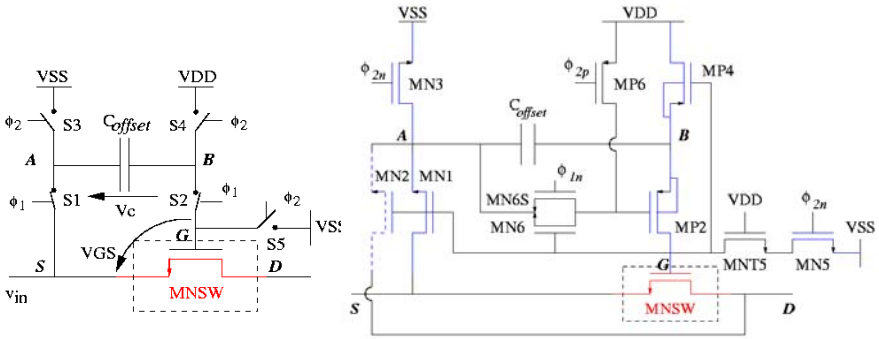



• Controlled overdrive of switch gate voltage:

$V_{GS} = V_{DD} - V_{SS}$

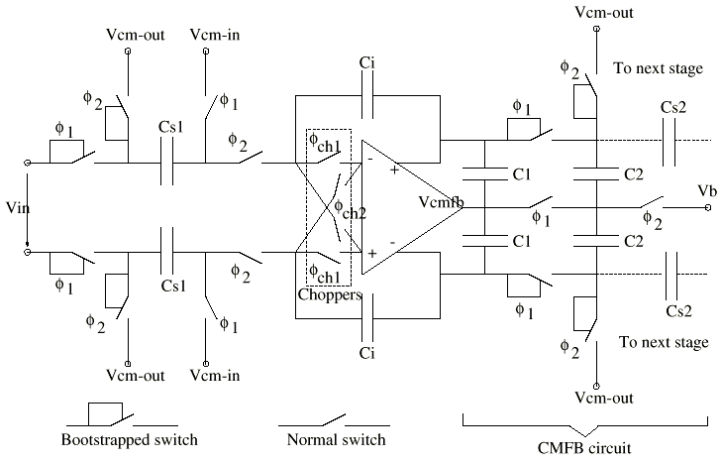


# Circuit implementation




• Fully compatible with LV technology !

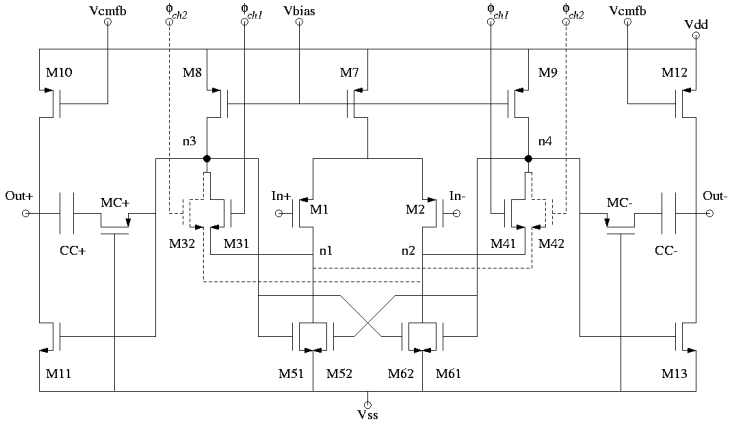
# ULV Integrator




Dessouky, Kaiser,ISCAS 2000



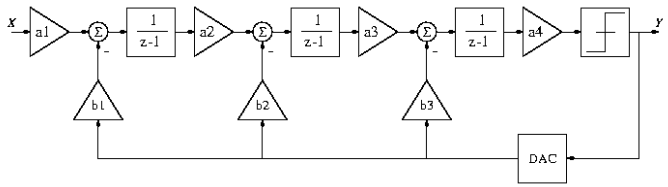
# ULV Amplifier Structure






# Low-Voltage Low-Power ΔΣ Modulator

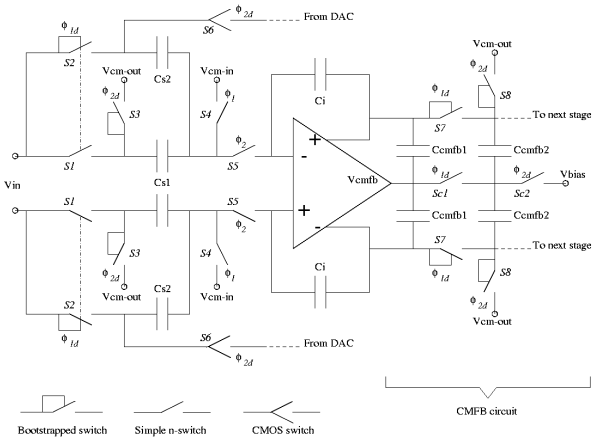
- Reducing VDD increases consumption! Thus ->:
  - Single loop for more relaxed requirements on the integrators.
  - High order to keep a low oversampling ratio.




Dessouky, Kaiser,CICC 2000

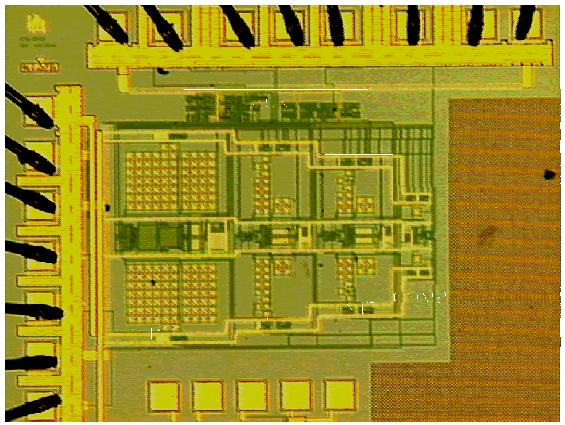


# Integrator structure




- Different input and output common-mode.
- Shared bootstrapped switches.

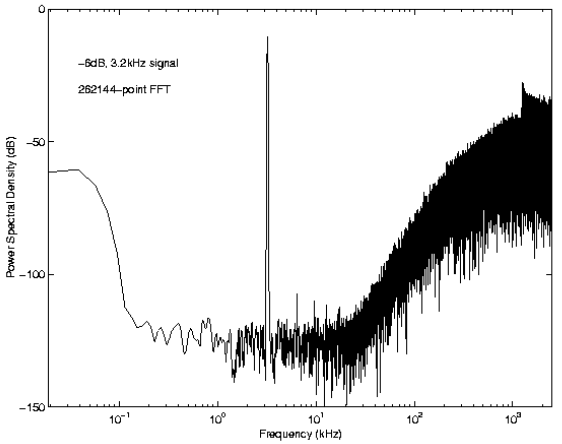
# ΔΣ Converter - Chip



Alcatel 0.35µ - TMDP  Area 0.9×0.7 mm²

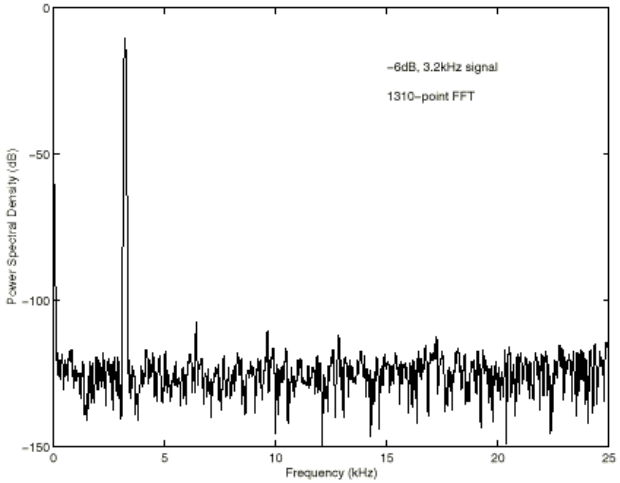


# Measured Results - PSD



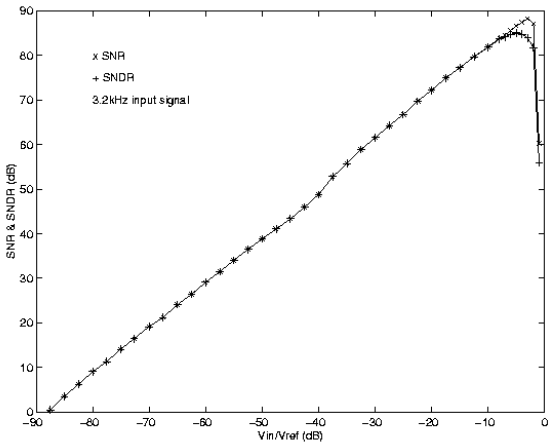



# Baseband Spectrum






# Measured Results - SNR/SNDR



# Measured Results - Summary

| | |
|---|---|
| **Supply Voltage** | **1 Volt** |
| **Reference Voltage** | **1 Volt** |
| **Dynamic Range** | **88 dB** |
| **SNR / SNDR** | **87 dB / 85 dB** |
| **Oversampling Ratio** | **100** |
| **Sampling Rate** | **5 MHz** |
| **Signal Bandwidth** | **25 kHz** |
| **Power Consumption** | **950 μW** |



# Measured Results - Comparison

| | Rabii_97 | Peluso_98 | Coban_99 | This work |
|---|---|---|---|---|
| Type | SC/VM | SO | SC/VM | SC/BS |
| VDD(V) | 1.8 | 0.9 | 1.5 | 1 |
| DR(dB) | 99 | 77 | 98 | 88 |
| SNDR(dB) | 95 | 62 | 88 | 85 |
| BW(kHz) | 25 | 16 | 20 | 25 |
| P(uW) | 2500 | 40 | 1000 | 950 |
| 4kTxDRxBW/PWR | 1316 | 330 | 2091 | 275 |