Adiabatic Logic Circuit for Biomedical Applications

Prepared by:

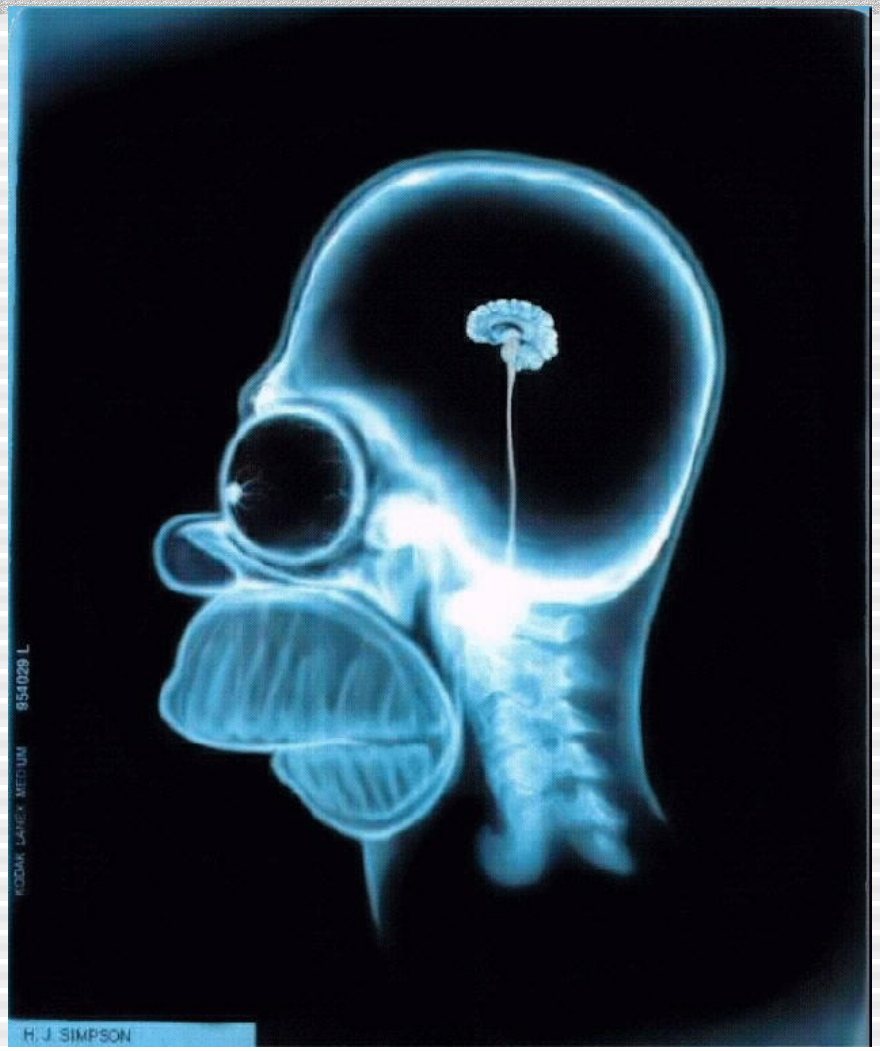
Muhammad Arsalan

Presented to:

Dr. Maitham Shams

Contents

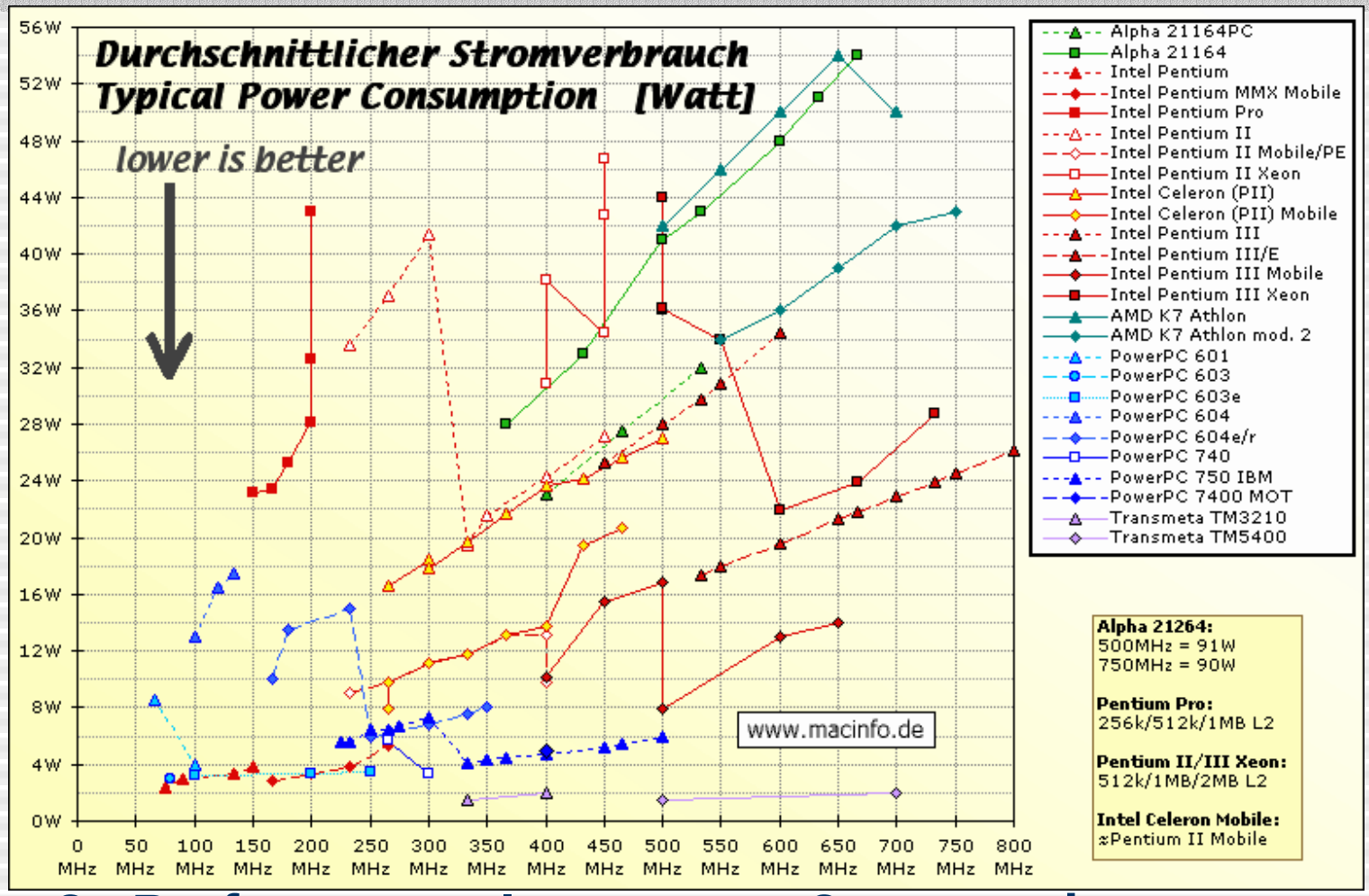
Low Power



Why Low Power?

- Heat dissipation is a big problem .
- Variation of device parameter and performance with temperature change
- Will become the bottleneck of the design.

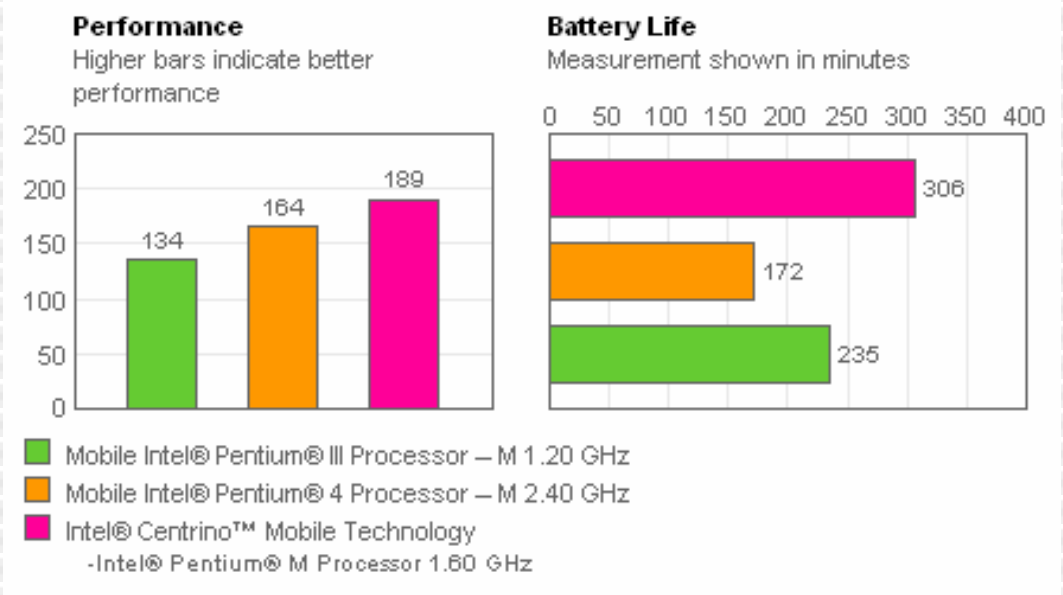
Power Dissipation of μPs



2x Performance Increase ⇒ 2x power increase

Low Power Techniques

- 2.8 GHz Pentium 4 - 68.4 W
- 2.2 GHz Mobile Pentium 4 - 30 W
- 733MHz PowerPC 7445 - 10 W
- Exception!!



Low Power Techniques

- *General Good Design Practices*
- *Process shrink*
- *Voltage scaling*
- *Transistor sizing*
- *Clock gating/transition reduction*
- *Power down testability blocks when not in the test mode*
- *Power down the functional blocks*
- *Minimize sequential elements*
- *Check for any slow slope signals in your design and fix them accordingly*
- *Downsize all non-critical path circuits*
- *Reduce loading on the clock*
- *Parallelism*
- *Adiabatic circuits*

Why Adiabatic Logic?

- *Difficulties in removing heat from high-speed VLSI circuit*
- *Battery-operated applications – portable devices*
- *Energy usage restriction*

- *Lower switching noise*

Power Dissipation in Conventional CMOS Inverter

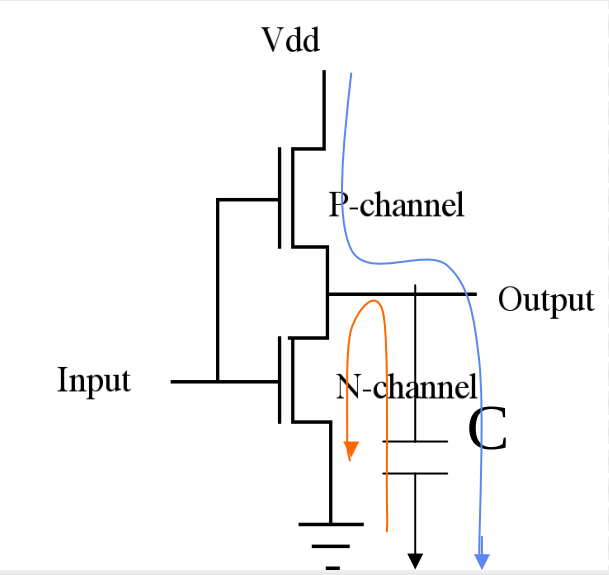
- DC power supply
- When input is low, energy drawn:

$$E = CV^2$$

- Energy stored in capacitor:

$$E = (1/2)CV^2$$

- When input is high, half of energy lost!



Power Dissipation in Adiabatic

- Depends on configuration, will see in soon in this presentation

Contents

What is Adiabatic Switching?

- Adiabatic switching is also called energy-recovery
  - “Adiabatic” describe thermodynamic reversible process that exchanges no heat with the environment
- Keep potential drop switching device small
- Allow the recycling of energy to reduce the total energy drawn from the power supply

Adiabatic Logic

- ***A universal adiabatic logic gate must include the following components:***
  - ***(1) The generalized spring which may undergo deformation caused by a driving force from the driver;***
  - ***(2) The switch which determines a logic transition in response to the driving force, depending on the input information;***
  - ***(3) The communication channel through which state information can be conveyed to other gates.***

Requirements for Adiabatic Logic

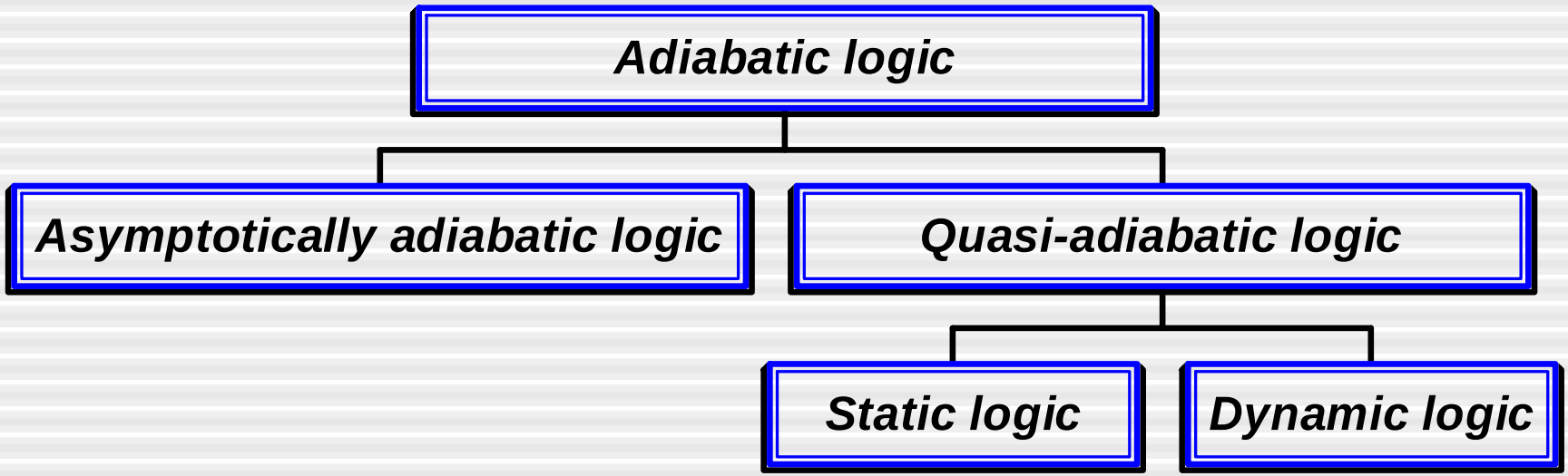
- ***Requirement A:***
  - ***The voltages between current-carrying electrodes must be zero when the transistors switch to the on state. Otherwise, some of the energy that has been accumulated by C will be dissipated.***

- ***Requirement B:***
  - ***The conductive coupling between the capacitor C and the driver must exist at any time. This is not the case in dynamic gates, in which the generalized***

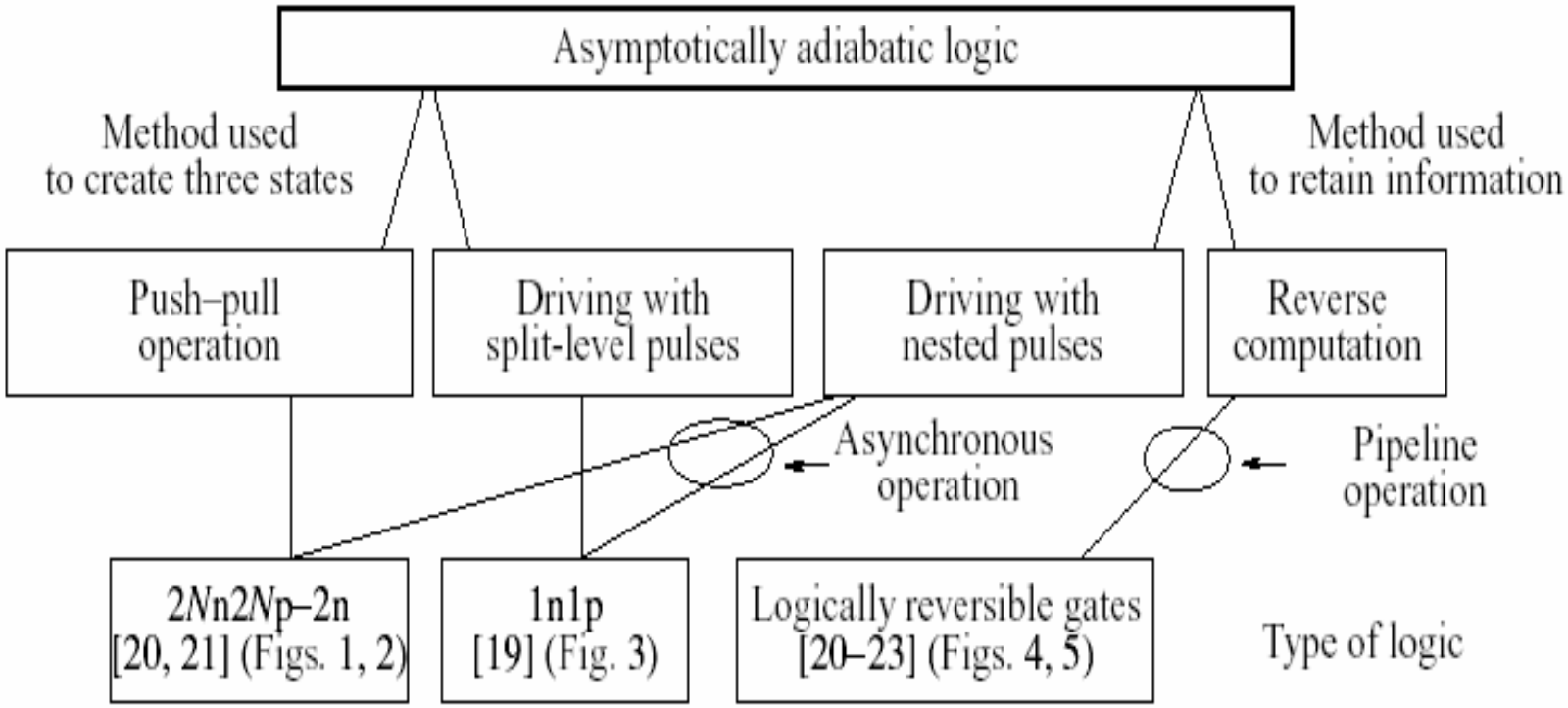
Classification of Circuits

- Rank-3: Asymptotically Adiabatic Logic
- Rank-2: Quasi Adiabatic Logic
  - $E=CV_{th}^{2}$
- Rank-1: Diode Charging Logic
  - $E = CV_{dd}V_{tD}$
- Rank 0: Conventional CMOS
  - $E = CV_{dd}^{2}$

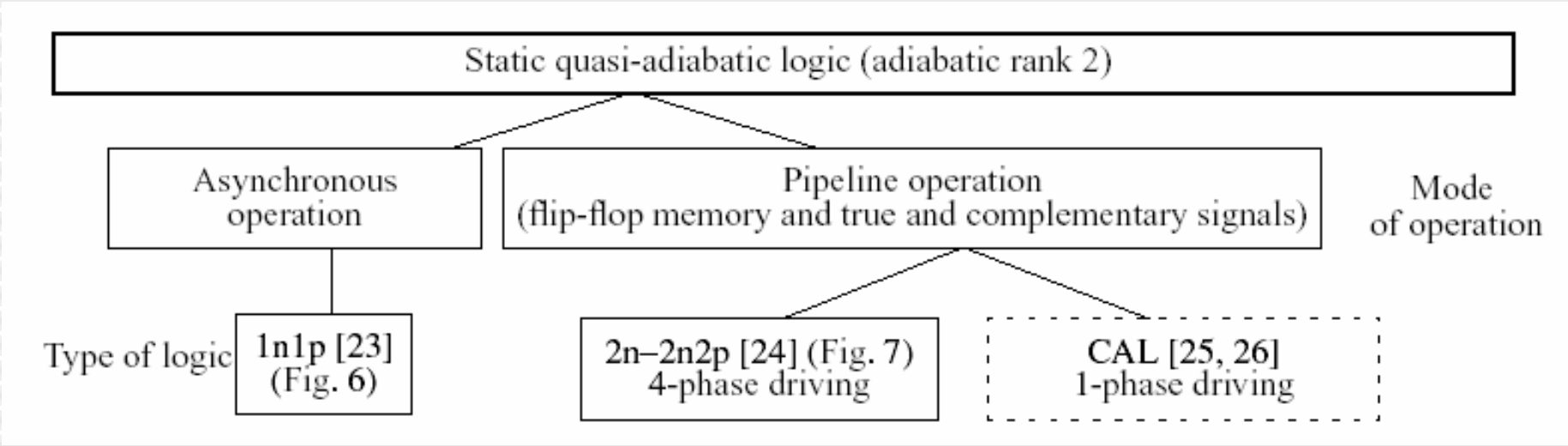
Classification of Adiabatic Circuits



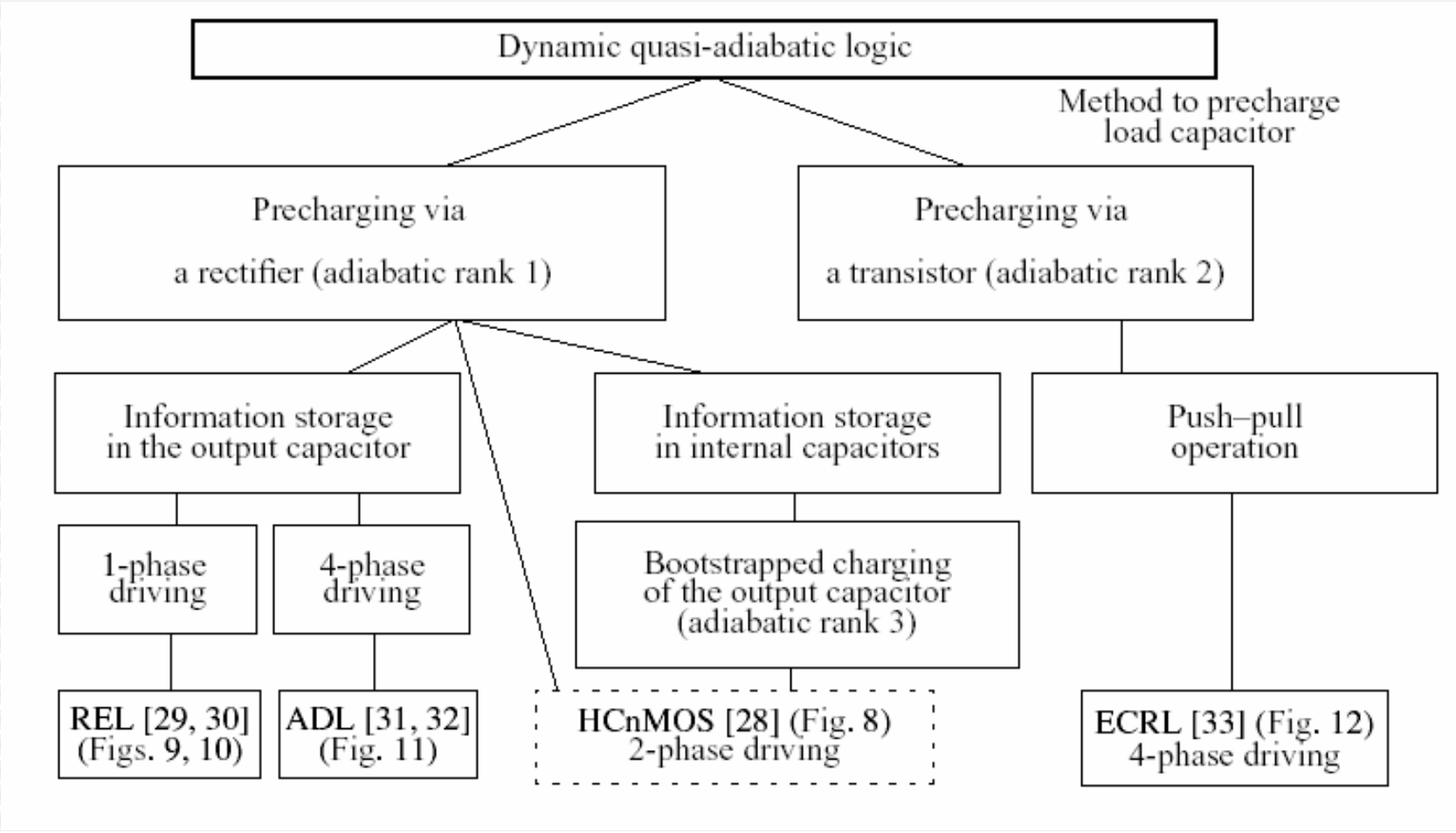
Classification of Adiabatic Circuits



Classification of Adiabatic Circuits



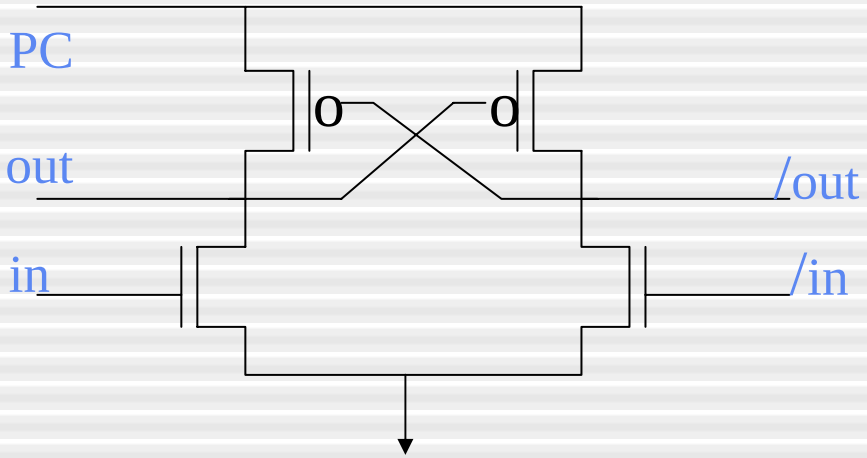
Classification of Adiabatic Circuits



Adiabatic Families

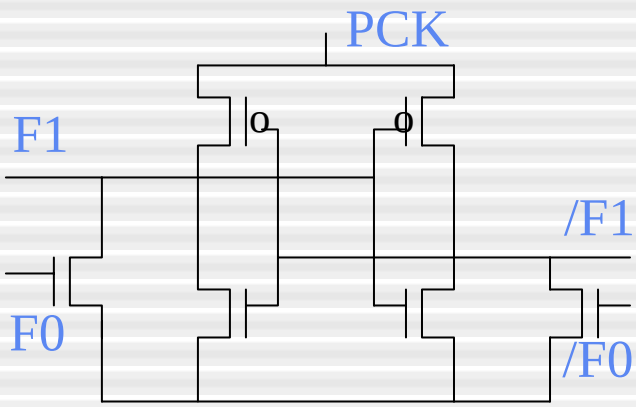
- ***Partially Adiabatic Logic***
  - ***2N2P / 2N-2N2P***
  - ***CAL (Clocked CMOS Adiabatic Logic)***
  - ***TSEL (True Single Phase Adiabatic)***
  - ***SCAL (Source-coupled Adiabatic Logic)***
- ***Fully Adiabatic Logic***
  - ***PAL (Pass-transistor Adiabatic Logic)***
  - ***Split-level Charge Recovery Logic (SCRL)***

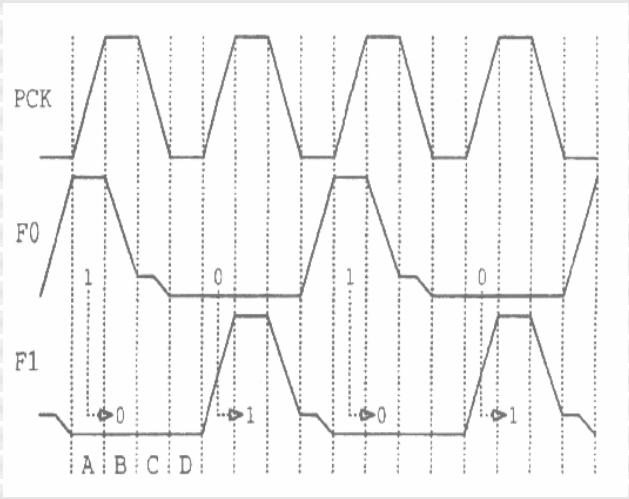
2N2P Inverter



2N2P Inverter

2N-2N2P Inverter



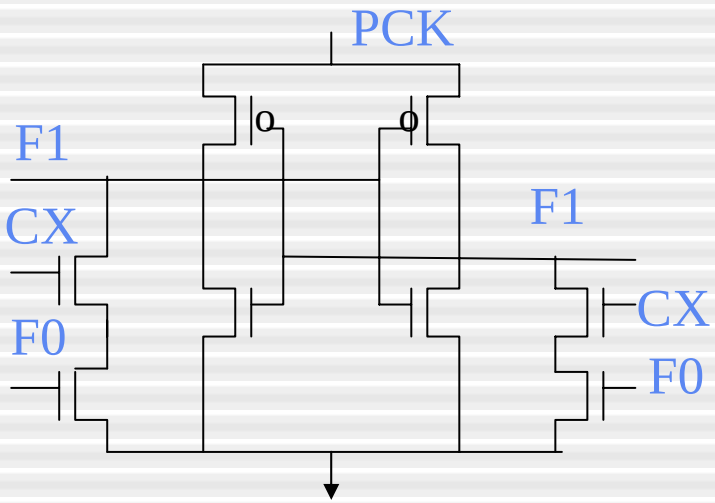


2N-2N2P Inverter

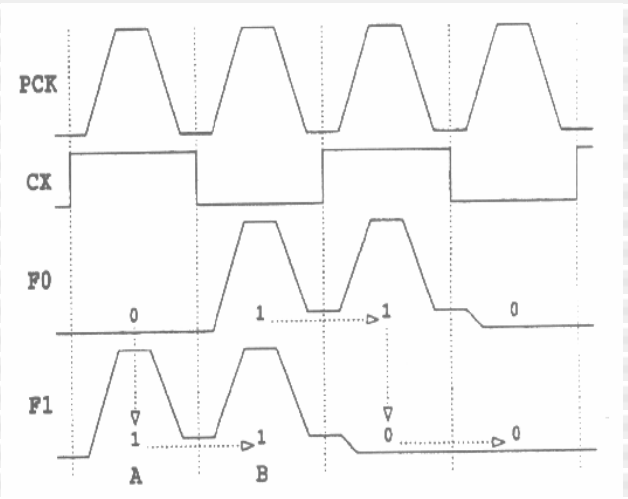
Signal waveform

CAL Inverter

- Cascades require single-phase clock and two auxiliary square-wave clocks



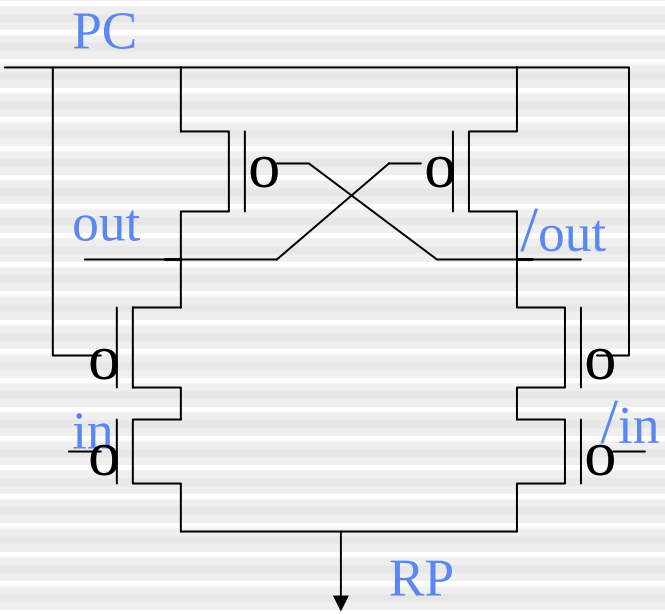
CAL Inverter



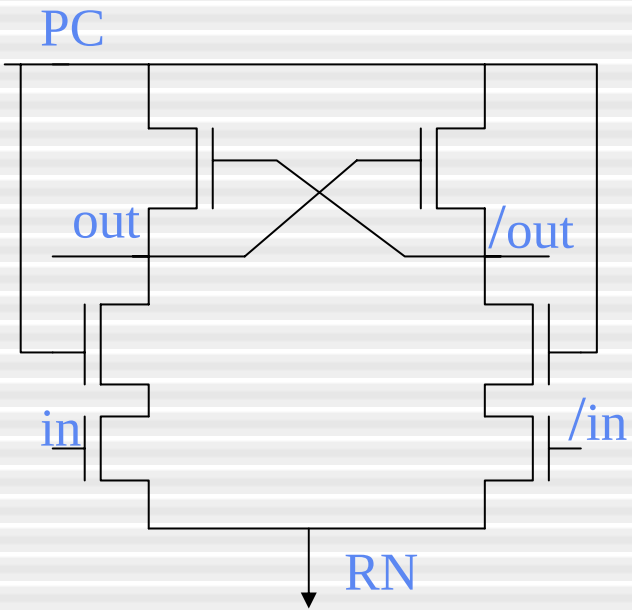
Signal Waveform

TSEL Inverter

- Cascades require single-phase sinusoidal power clock
- Two DC voltages ensure high-speed operation



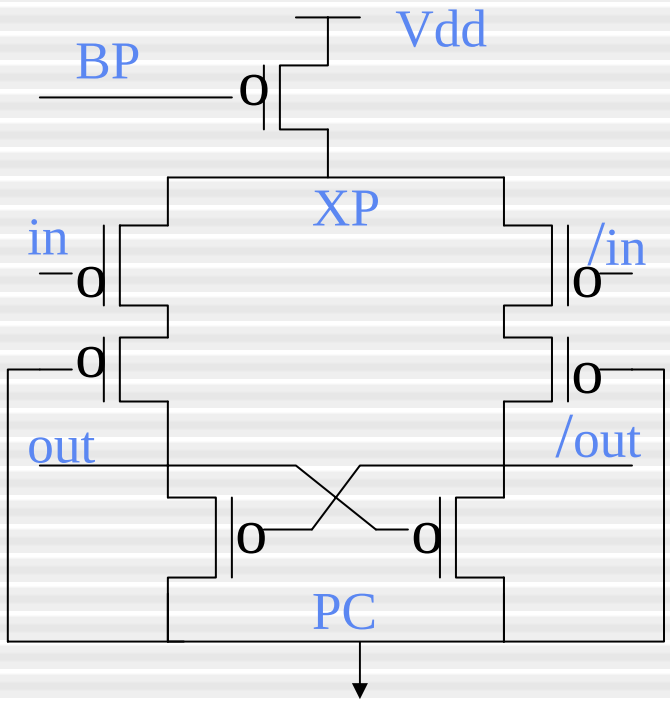
PMOS TSEL Inverter



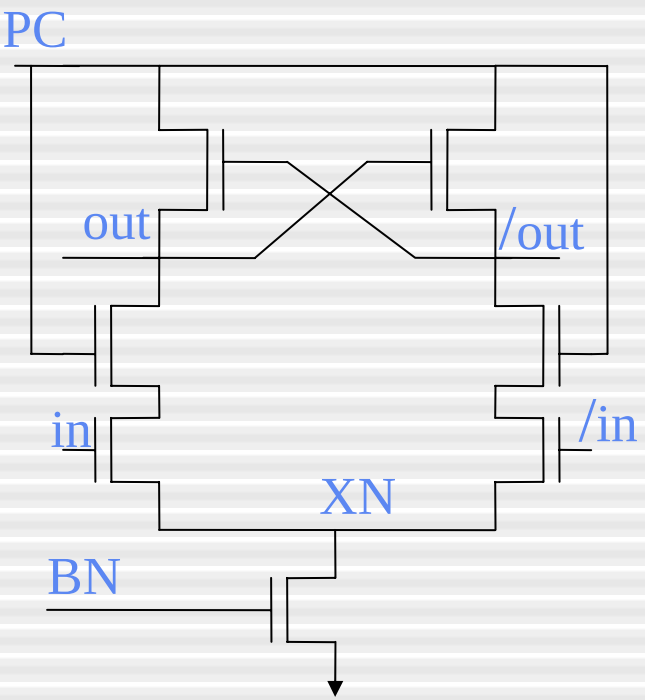
NMOS TSEL Inverter

SCAL Inverter

- Cascades require a single controller power clock
- Speed can be tuned individually



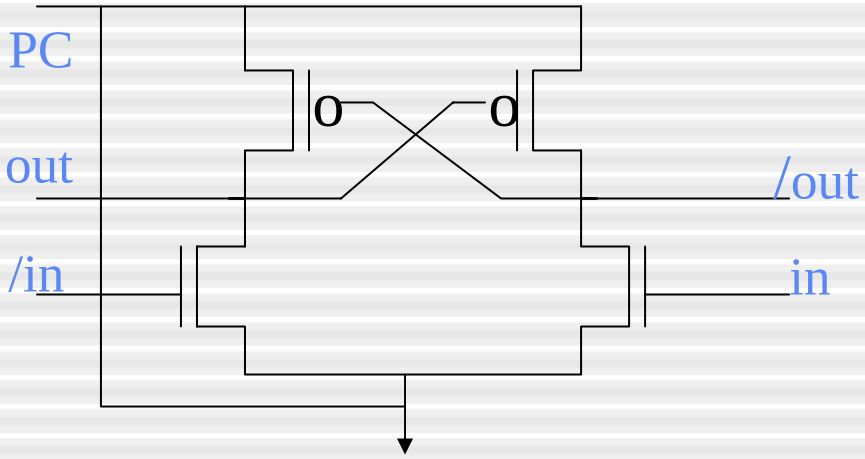
PMOS SCAL Inverter



NMOS SCAL Inverter

PAL Inverter

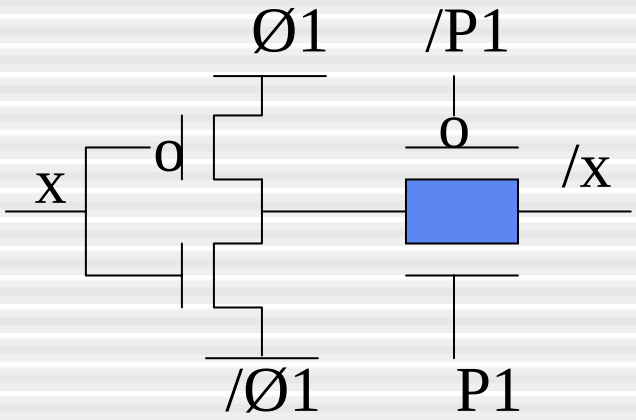
- Cascades require two-phase clock
- Fully adiabatic at the cost of high speed



PAL Inverter

SCRL

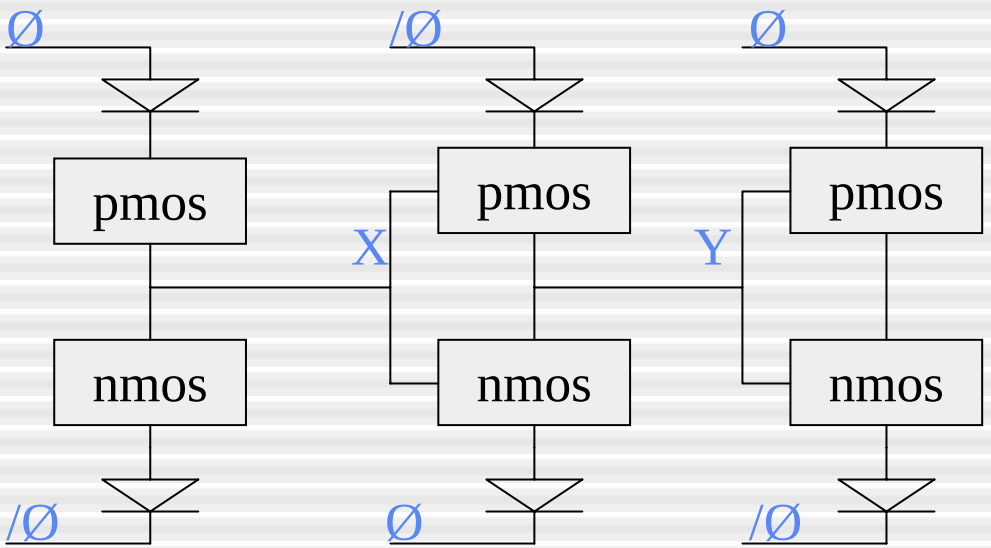
- Split-level Charge Recovery Logic (SCRL)

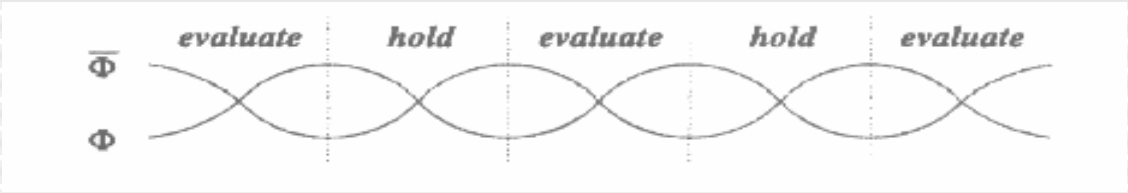


SCRL version of Adiabatic Buffer

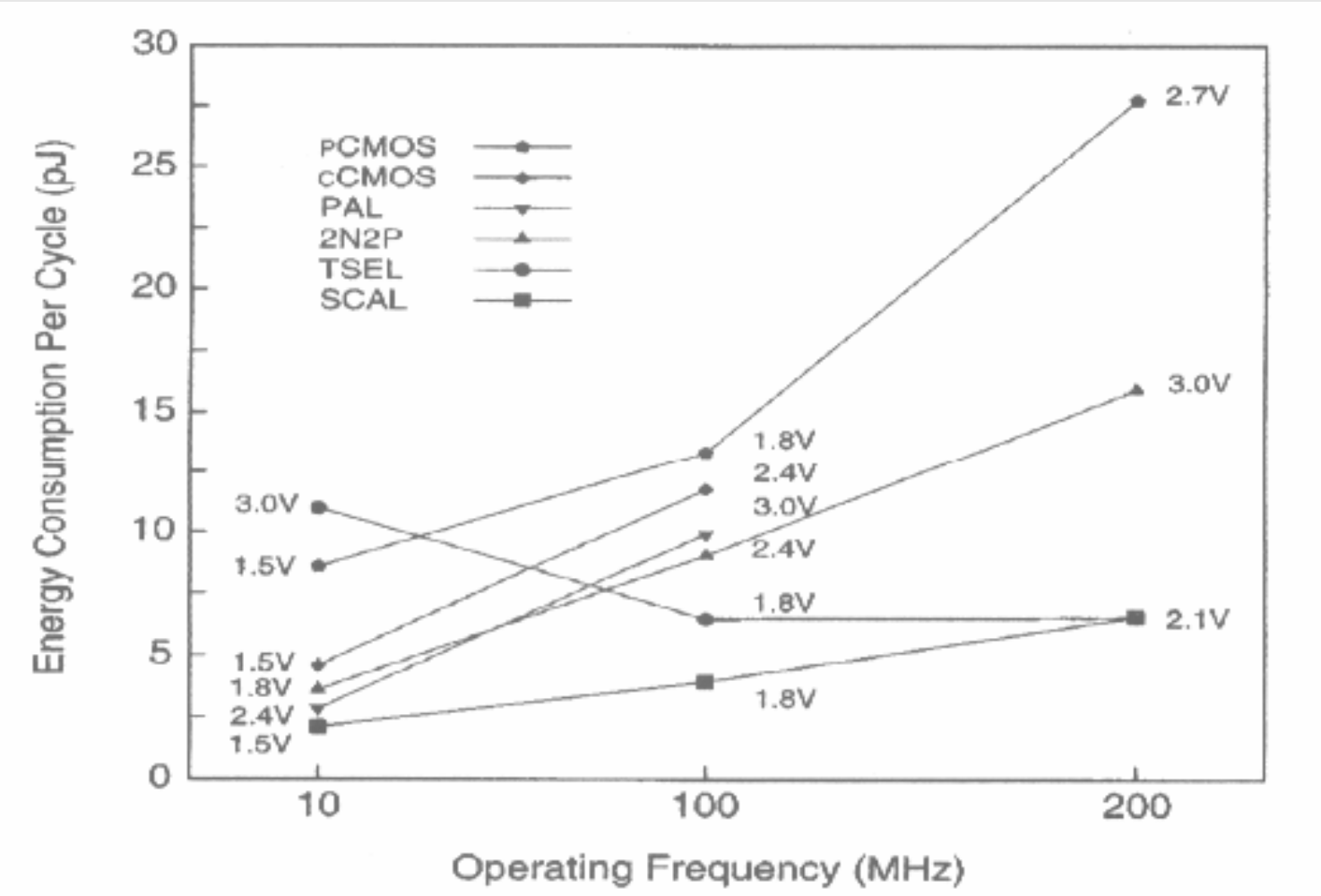
QSERL

- Quasi-Static Energy Recovery Logic (QSERL)





Energy Consumption

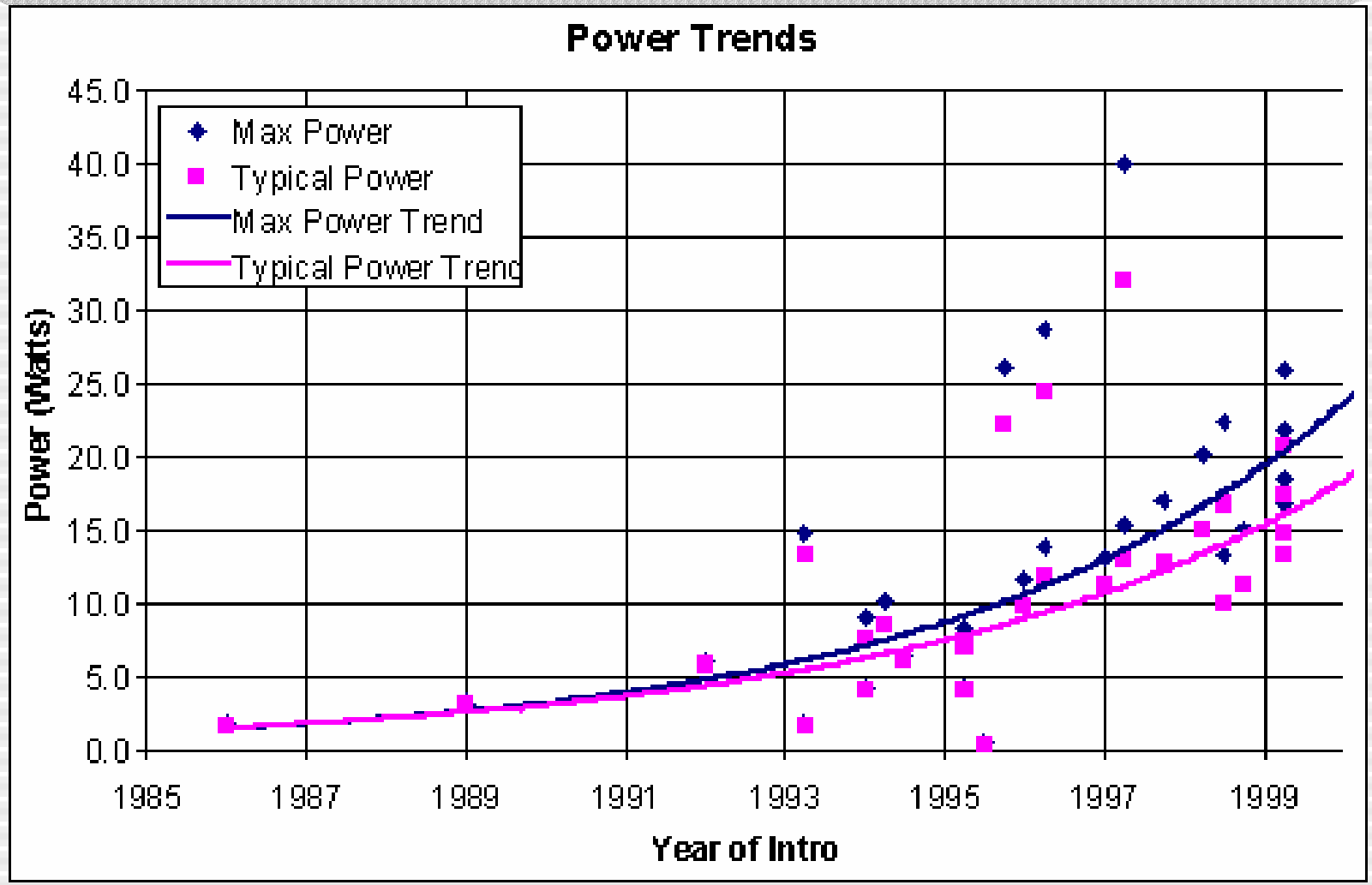


Technology Tradeoffs

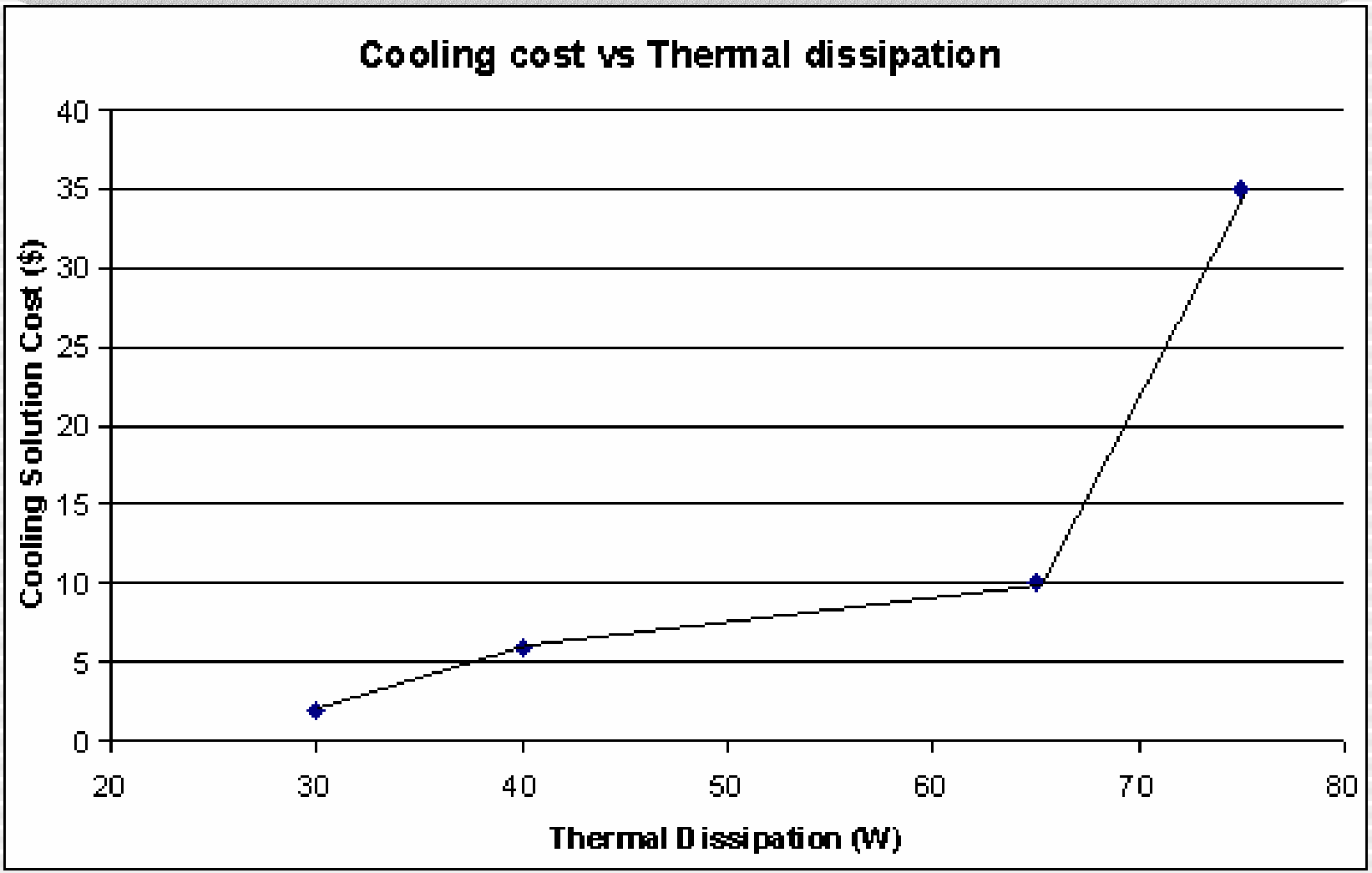
- ***Advantages***
  - ***Energy saving of 76% to 90%***
  - ***Two-order of magnitude reduction in switching noise***
- ***Disadvantages***
  - ***Lower-speed operation, for example, the experiment frequency is only up to 200MHZ***
  - ***Larger Circuit Area***
  - ***Memory Requirements***

Future Trends

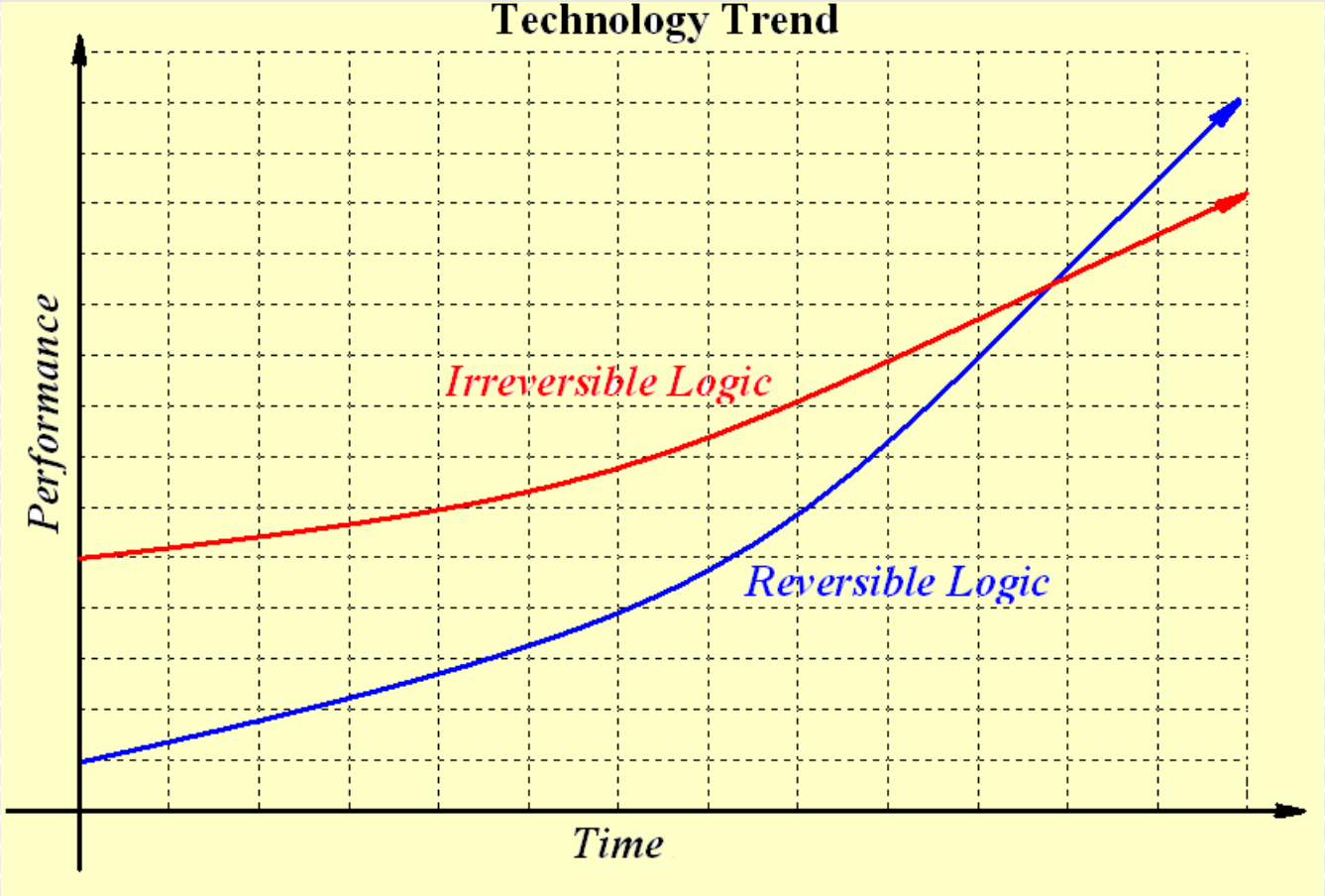
Future Trends



Future Trends



Future Trends

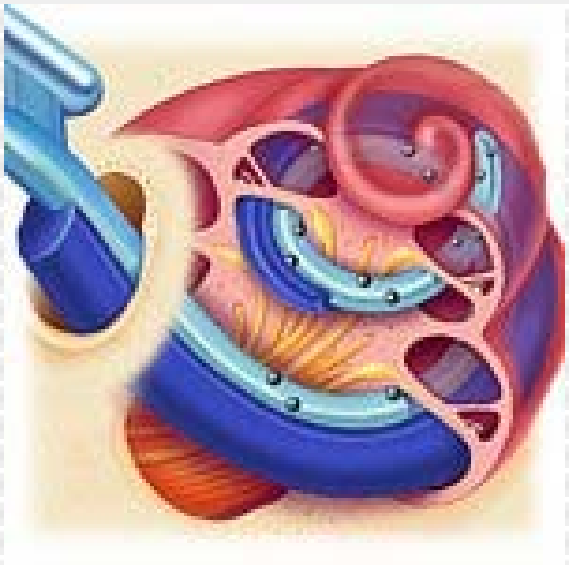


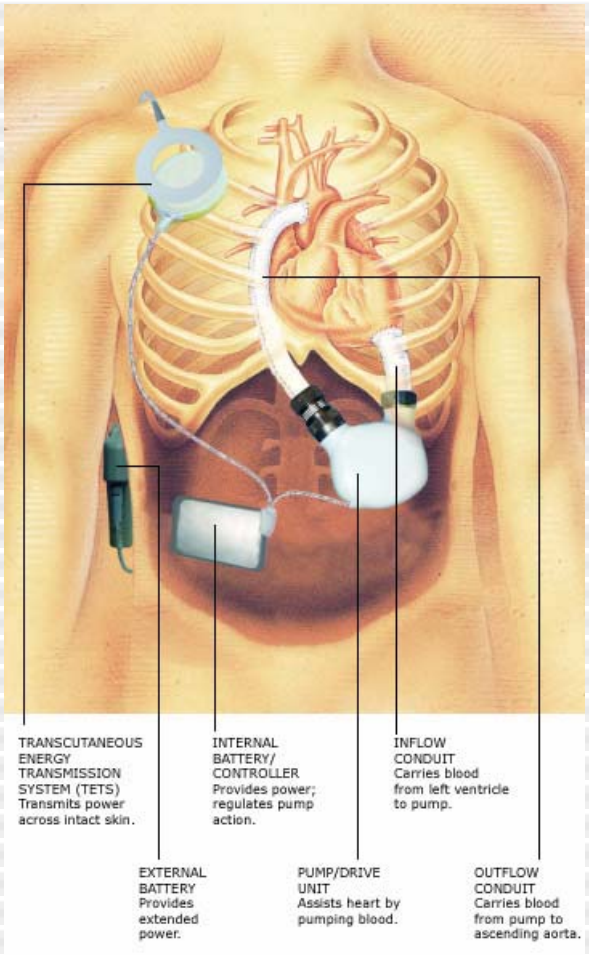
Contents

Applications

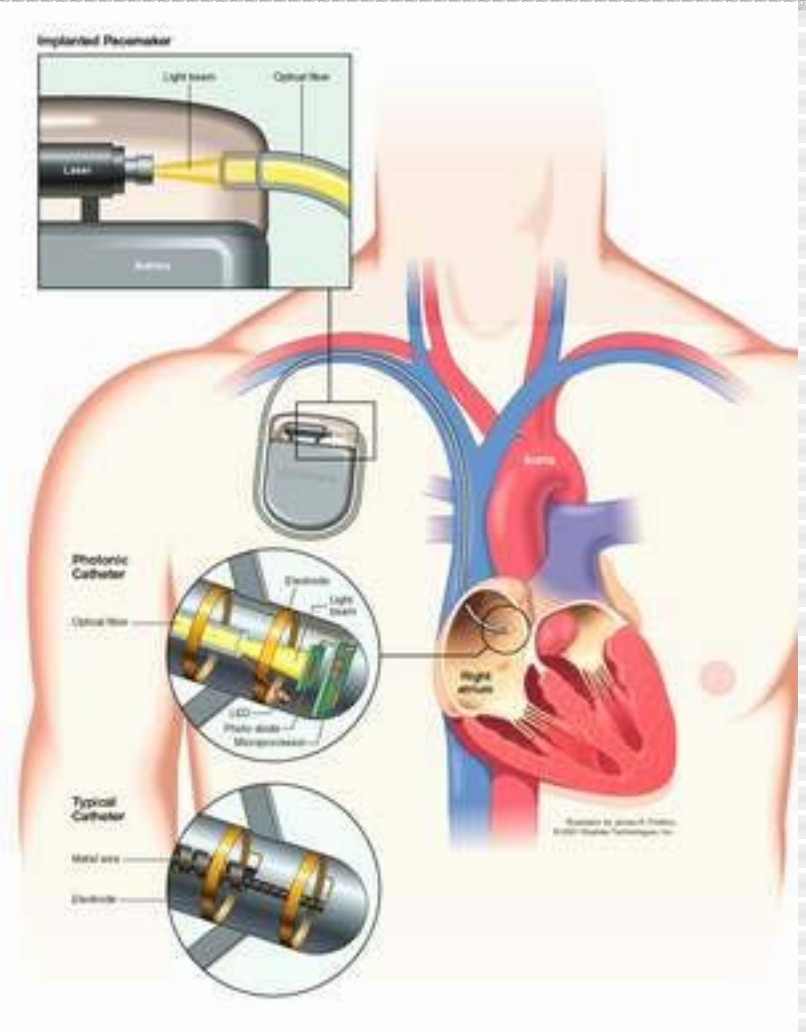
- ***What would be the applications of such a device?***
  - ***Automated deep-space probes travelling far from the sun, hence no solar power.***
  - ***Personal portable computers.***
  - ***Data Gathering devices undersea or underground.***
  - ***Medical implants with human body.***

Medical implants

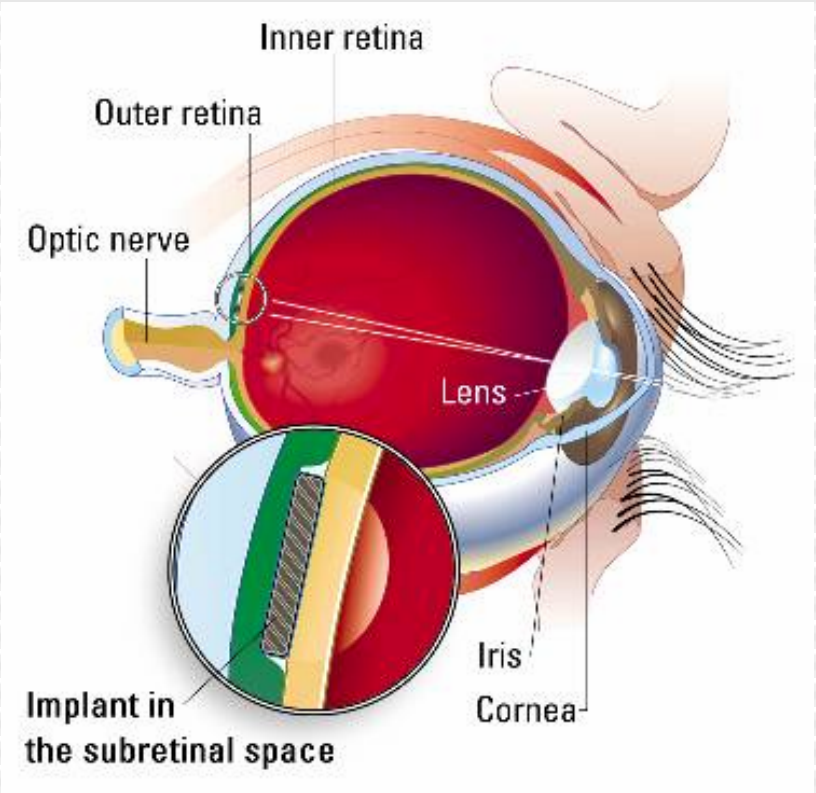


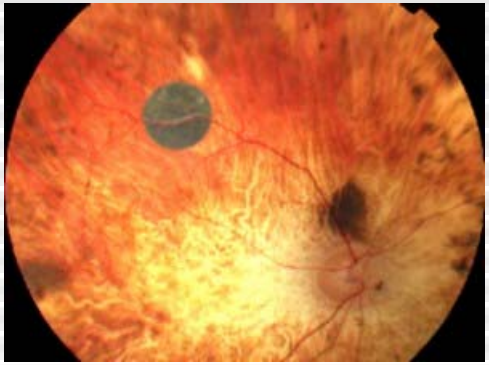


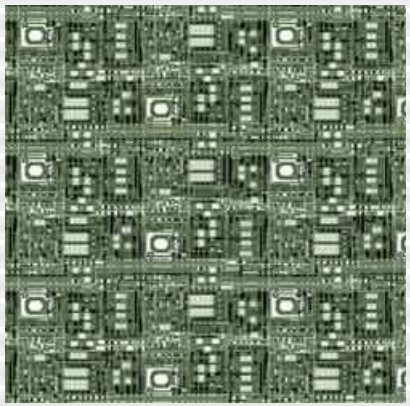
Medical implants



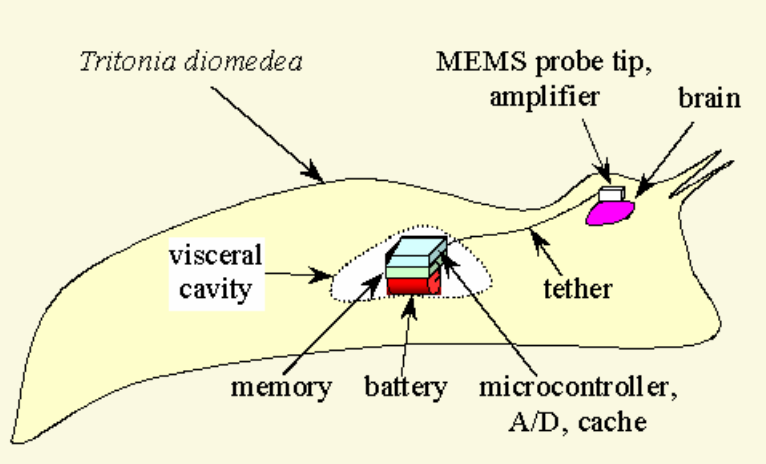
Medical implants





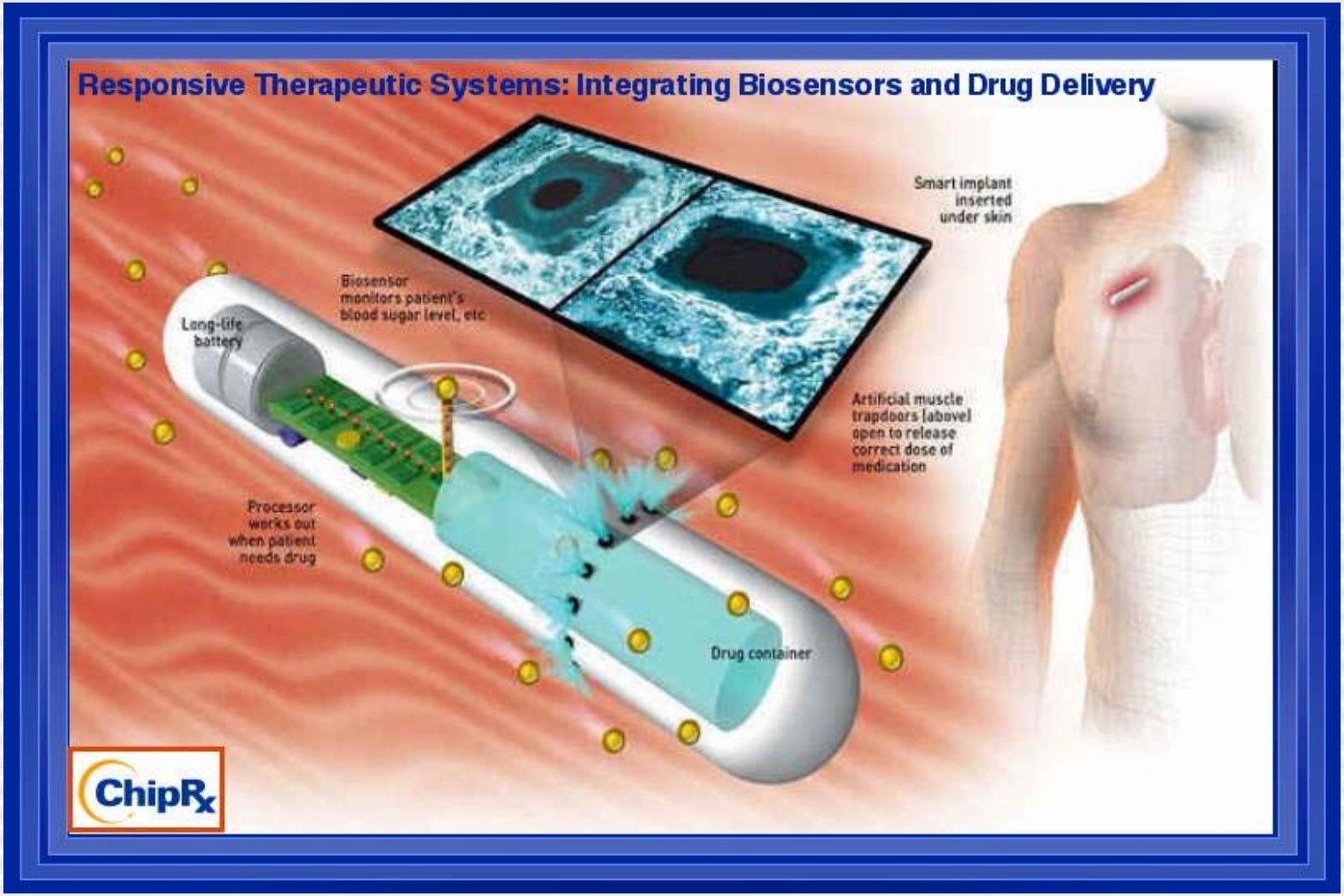


Medical implants

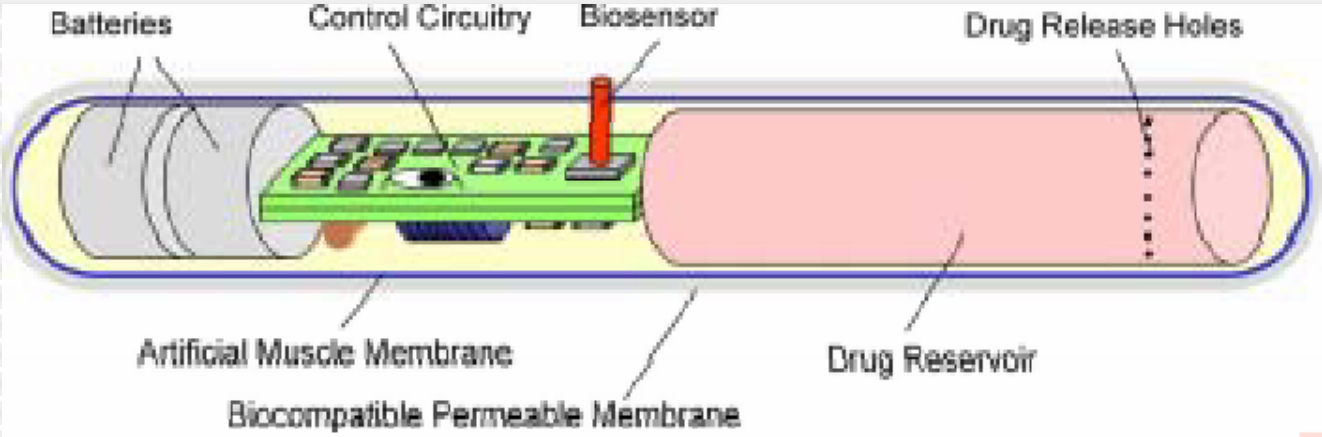


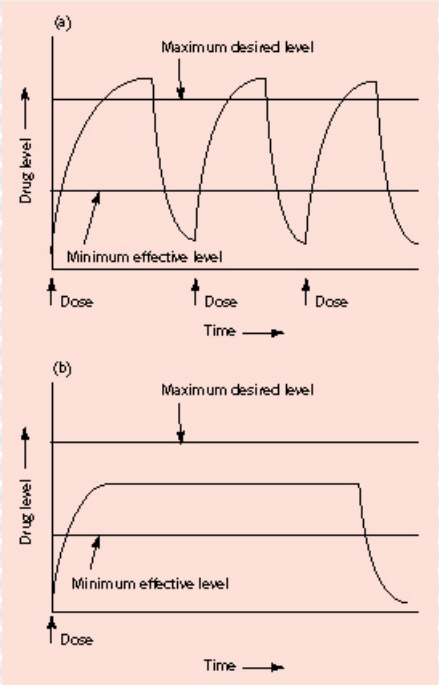
Intracellular neuronal recording system: Stand-alone implantable microsystem with probe tips, amplifier, signal compression, and data storage.

Medical implants

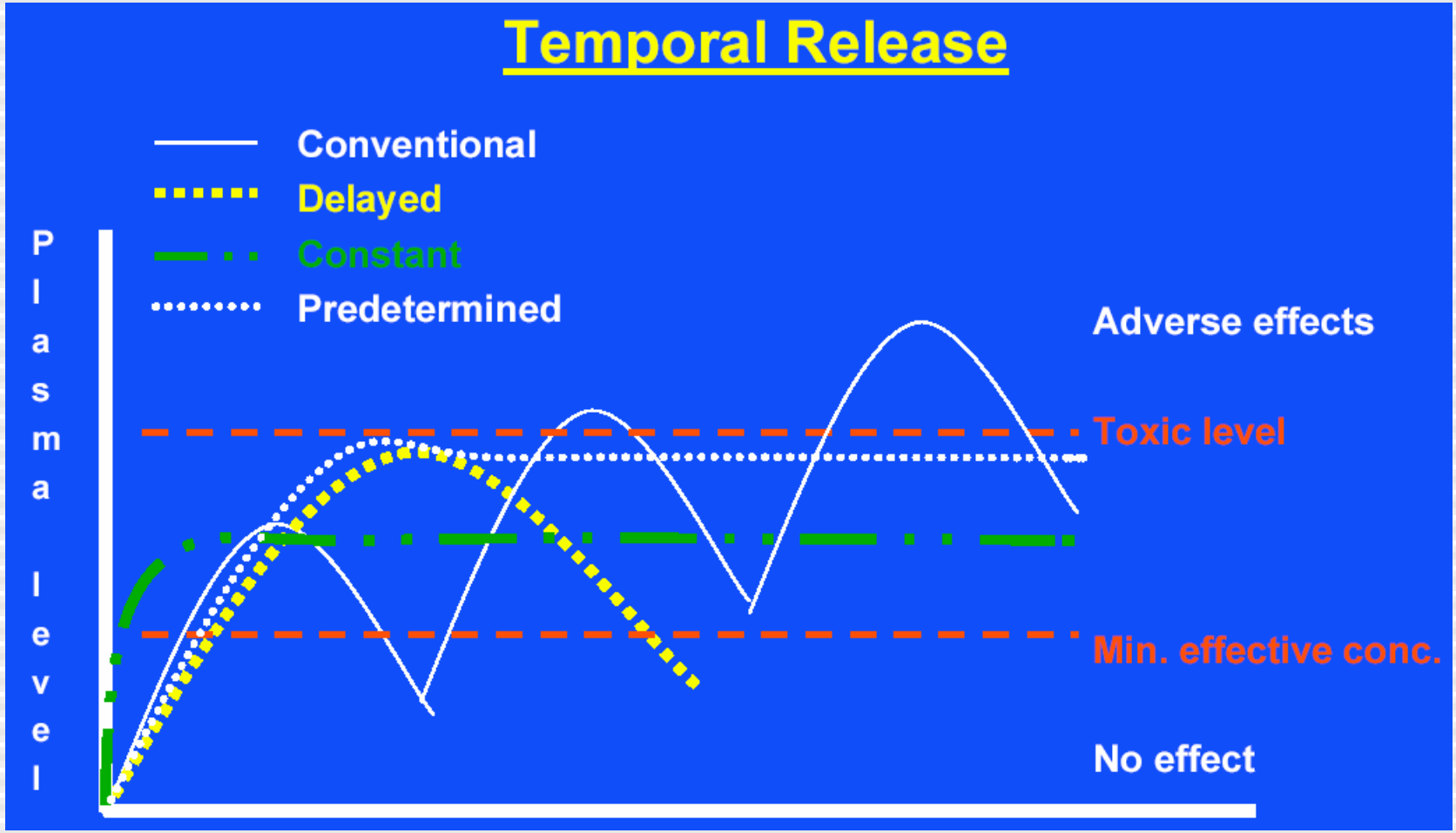


Responsive Drug Delivery

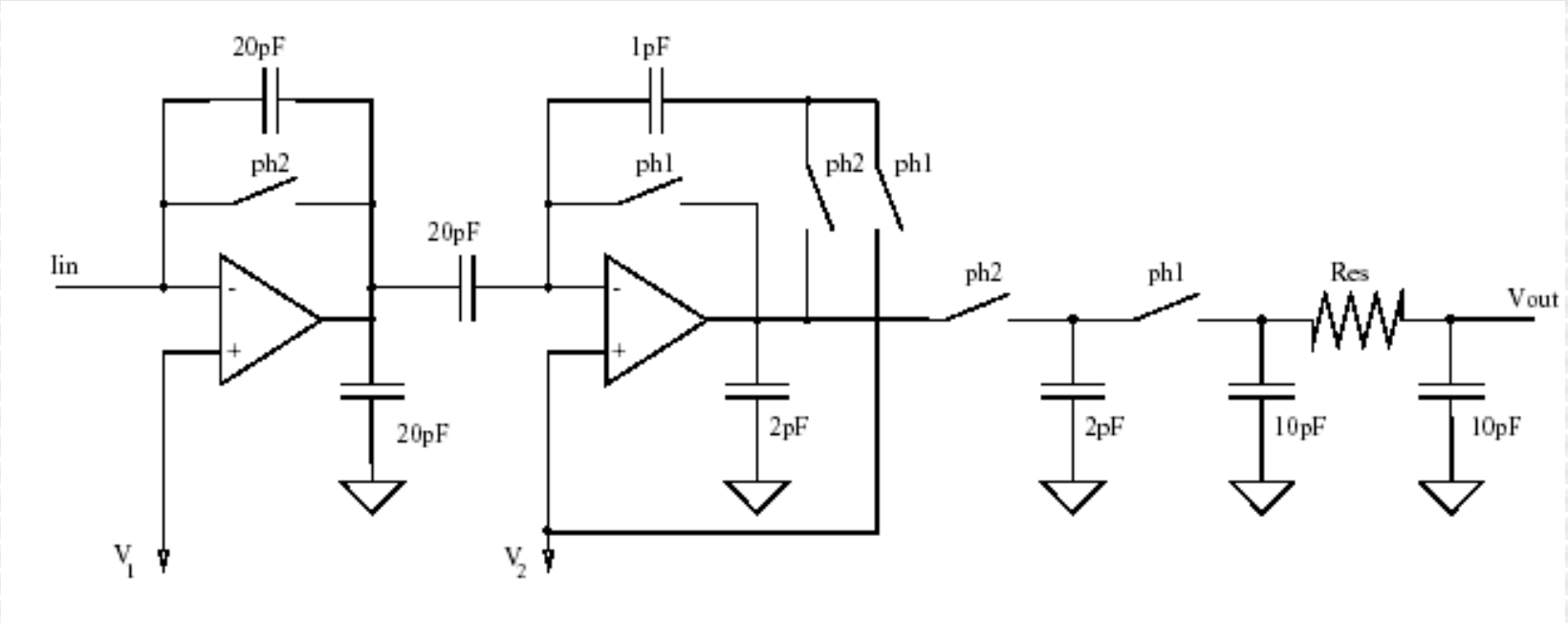




Low Power Techniques



CMOS Current Amplifier for Biological Sensors



Proposed Project Schedule

S#	Description	From	To
1	Final Decision for Application	-	March 31st
2	Initial Test & Development	April 1st	April 14th
3	Design & Simulations	April 15th	April 27th
4	Project Presentation	-	April 28th
5	Final Report	April 29th	May 5th

References

- A CMOS Current Amplifier for Biological Sensors, Piper, J. et al., Dept. of Applied Electronics, Lund University.
- Anantha P.C. & Robert W.B., Low Power Digital CMOS Design
- M.P. Frank, Low Energy Computating for Implantable Medical Devices, MIT, 1996
- X. Wang & U. Hashmi, Adiabatic Switching
- V.K. De & J.D. Meindl, A dynamic Energy Recycling Family for Ultra Low Power, 1996
- A. Kramer & J.S. Denker, Adiabatic Computing with 2N-2N2D Logic Family, 1994
- L.A. Akres & R. Suram, Adiabaic Circuits for Low Power Logic, 2002
- S. Kim & M. C. Papaefthymiou, Single-Phase Source Coupled Adiabatic Logic, 1999
- X. WU, X. Liu & J Hu, Adiabatic NP-Domino Circuits, 2001
- Athas, W.C., Svensson, L.J., Koller, J.G., Tzartzanis, N.,and Chou, E.Y.-C., Low-Power Digital Systems Based on Adiabatic-Switching Principles, 1994
- Ferrary, A., Adiabatic Switching, Adiabatic Logic, 1966.
- Younis, S.G. and Knight, T.F., Asymptotically Zero Energy Split-Level Charge Recovery Logic, Proc. 1994

Thank You!