

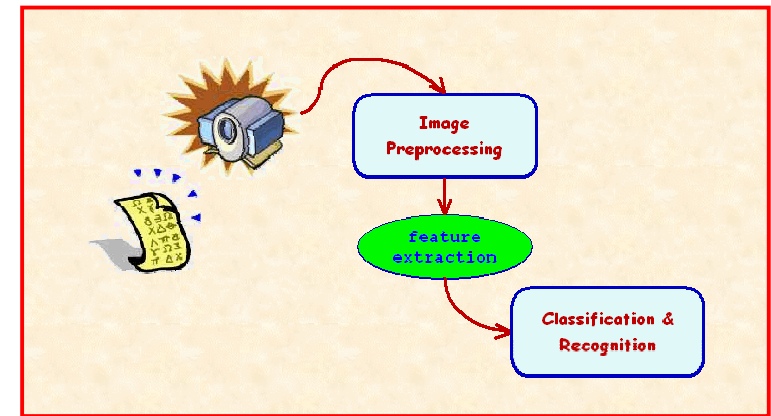
## Two exemplary applications:

- Optical Character Recognition Systems
- Digital communication channels adaptive equalization



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## OCR System Architecture



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Low Power Design Techniques and Neural Applications  
Barcelona, Feb. 23-27 2004

Applications

1

## Portable OCR Systems



☉ Pen scanners with OCR capabilities are emerging as a new segment of portable equipments

⇒ They can still be improved in:

- ♣ robustness against variations of fonts, contrast and hand speed
- ♣ recognition of symbols, punctuation and handwriting
- ♣ speed
- ♣ accuracy
- ♣ power efficiency
- ♣ connectivity
- ♣ etc.

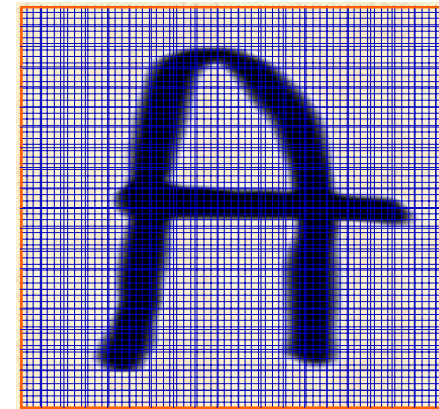
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Applications

2

## Image definition for handwriting



$20 \times 20 = 400$  pixels

$64 \times 64 = 4096$  pixels

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Applications

3

## OCR Chip Examples

- **1992: ANNA Neural Network Chip**  
by E. Säcker, et al. - AT&T  
IEEE - Trans. NN's, Vol. 3, No. 3
- **1998: Analog VLSI Feature Extractor**  
by G.M. Bo, et al. - DIBE  
IEEE - JSSC, Vol. 33, no. 3
- **1999: 10 mW CMOS Retina and Classifier**  
by P. Masa, et al. - CSEM  
IEEE - ISSCC, 15-17 Feb. 1999

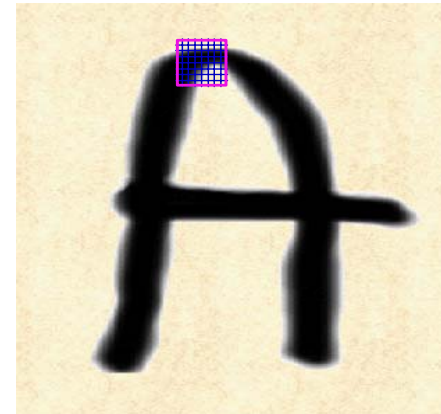
20 × 20

32 × 24

32 × 20

## Representation of handwriting

8 × 8 = 64 pixels



- ⊙ Same definition as a 64 × 64 matrix

but

- ⊙ partitioned in a number of 8 × 8 sub-matrices

How many?

## OCR architecture (1)

Character ⇒ Scanner ⇒ Pre-processing ⇒ Feature Extractor ⇒ Classification

- **Feature Extractor**

Input Character: a matrix of 36 × 24 binary pixels preprocessed by a segmentation and a normalization block.

The matrix is partitioned into 16 subimages of 7 × 9 pixels partially overlapped. From each subimages 7 features are extracted. The overall number of features are 112. This feature evaluate the density of the active pixels in the considered subimage and the extension of the character shape in the six major directions.

- **Classification**

The feature obtained feed a neural classifier based on one or two coupled Multi Layer Perceptron network.

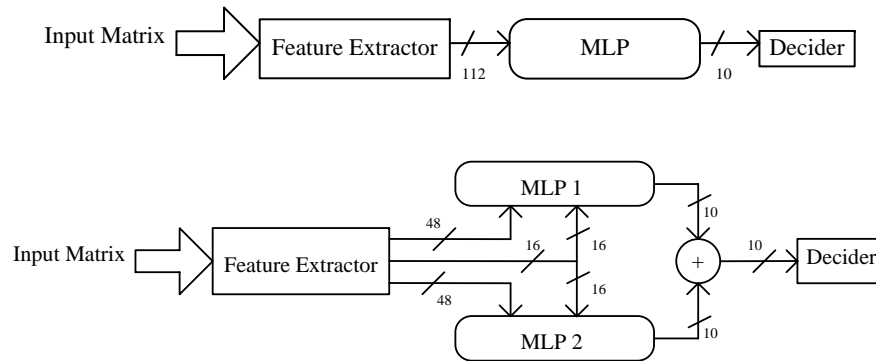
The training of the neural classifier can be achieved with a chip in the loop technique, in which the analog VLSI architecture performs the feedforward computations while the error computations and weights generation is performed by a digital host computer.

## OCR architecture (2)

OCR system based on analog computational modules  
and neural computational paradigms

<i>Feature Extraction:</i>	reduction of redundancy of information of input characters
<i>Neural Classifier:</i>	performance comparable/higher with respect to those obtained with statistical classifiers
<i>Coupled Classifiers:</i>	low error rate/low complexity (system partitioning)
<i>Analog VLSI:</i>	high speed, high parallelism, low area, low power consumption
<i>Current Mode Approach:</i>	low dependence on technological parameters variations and process gradients

## OCR architecture (3)



## OCR architecture (4): validation

Training data base: NIST Special Database 3. 30000 character for training set and 58646 for test set.

Simulations performed on the single MLP architecture and couple MLP architecture (the outputs of the coupled MLP are combined, averaging the corresponding outputs of the two modules).

	N	ER	NR	ENR
<b>Single MLP classifier</b>	350	3.35%	2.72%	4.74%
<b>Coupled MLPs classifier</b>	250+250	2.87%	2.52%	4.17%

N: average number of iterations (epoch presentations) for each training procedure;  
 ER: error rates with a rejection criterion of 20%;  
 NR: rejected samples with a rejection criterion of 20%;  
 ENR: error rates obtained with no rejection criterion.