# Adiabatic circuits

SOCRATES'04
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## Adiabatic circuits

Adiabatic circuits achieve low energy dissipation by restricting current to flow across devices with low voltage drop and by recycling the energy stored on their capacitors.

Adiabatic logic families

- Best behaviour in lower generation of switching noise
- Switching occurs with the minimum voltage drop across devices and nodes vootages changes slowly

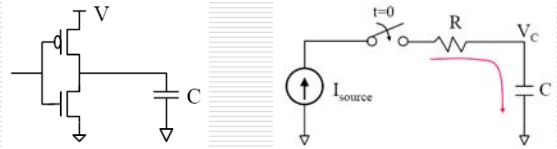


## Adiabatic circuits

- $E = Q \cdot V = C \cdot V^2$ → Energy drawn from the power supply during a 0 to V transition in an inverter with load C is given by
- Amount of energy stored in the output node (the energy stored in the output capacitance: only half the original)

$$E = \int_0^V C v_0 dv_0 = \frac{1}{2} CV^2$$

- Dissipation can be reduced minimising switching events, reducing voltage swing, decreasing capacitances, or apply a combination of these methods. But, in all the cases, the energy drawn by power supply is only once used.
- Adiabatic logic offers the possibility of further reducing the energy dissipated during switched events, and the possibility of recycling




**Charge-up event model for conventional CMOS circuits**



## Adiabatic circuits

In conventional CMOS circuits, the equivalent circuit used to model the charge-up event follows the expression

$$V_C(t) = \frac{1}{C} I_{source} t \rightarrow I_{source} = C \frac{V_C(t)}{t}$$

The amount of energy dissipated in the resistor R from t=0 to t=T can be expressed as

$$E_{diss} = R \int_0^T I_{source}^2 dt = R I_{source}^2 T = \frac{RC}{T} C V_C^2(T) \quad (1)$$

where can be glimpsed that if the charging time T is larger than $2 \cdot R \cdot C$, the energy is smaller than in the conventional case, and that the energy is proportional to the resistance R .

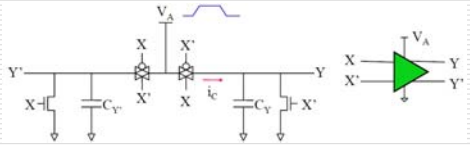
So, an *adiabatic charging* is necessary: reduction of the dissipation to an arbitrary degree by increasing the switching time to ever-larger values. The switching circuits that charge and discharge their load capacitance adiabatically are called *adiabatic switching circuits*

The circuits rely on special power supplies that provide accurate pulsed-power delivery, and are useful only if power supplies can deliver power efficiently and recycle the power fed back to them

# Adiabatic amplifier

## Adiabatic amplifier

- It is a simple buffer circuit that uses adiabatic charging to drive a capacitive load.
- It can be used a stand-alone circuit as a line-driver for an address bus on a memory board.
  - Equation (1) assumes CL charged/discharged through a constant resistance. As a first approximation, it can be applied to a linearised CMOS transmission gate.




  - For small voltage drop across the gate (intended in adiabatic circuits), conductances are modeled as (with $V_{avg}$ being the average voltage of the channel):

$$G_p = \frac{C_p}{K_p}(V_{avg} - V_t) \qquad G_n = \frac{C_n}{K_n}(V_{dd} - V_{avg} - V_t)$$

  - Selecting widths such that $K_n/C_n = K_p/C_p$, then the on resistance of the T-gate is

$$G_p + G_n = \frac{C_n}{K_n}(V_{dd} - 2V_t) \Rightarrow \quad Rtg = \frac{K_n}{C_n(V_{dd} - 2V_t)} \quad (2)$$

formulation that assumes that both devices are conducting, which is not the case when one voltage is at supply rail but. However, as in the extremes the on-resistance will be less than calculated, it will represent a worst case value.



# Adiabatic amplifier

## In the adiabatic amplifier

- inputs and outputs are dual rail encoded (neediness of both signal polarities to control T-gates),
- what makes capacitive load seen by the power supply data independent

## Amplifier operation:

- First the input is set to a valid value
- Next, the amplifier is energysed applying to $V_A$ a slow input voltage ramp from 0 to $V_{dd}$. With a slow ramp (in respect to $R_{tg}C_L$), one of the ramps will be adiabatically charged through one of the T-gates. The valid output signal is used as inputs to other
- Then, the circuit is de-energysed by ramping the voltage on $V_A$ back to 0. The signal energy stored into the load capacitance flows back to the power supply connected to $V_A$, recycling the power supply the returned energy.

## Using (1) and (2) can be found the energy efficiency of the amplifier.

- $E_{load}$ is the dissipation caused directly charging and discharging the load capacitance, where $\xi$ accounts for the non-constant shape factor charge current (equal to $\pi^2/8$ for a sine-shaped current)
- Analysis is simplified supposing the total input capacitance negligible in front of the effective load
- Ein represents the energy dissipated driving the input capacitance (supposing inputs driven conventionally to VDD)
- Total input capacitance proportional to the gate capacitance with constant proportionallity $\alpha = (C_p + C_n)/C_n$
- Then

$$E_{total} = E_{in} + E_{load} = \alpha C_n V_{dd}^2 + \frac{2\xi}{T}\frac{Kn}{C_n(V_{dd} - 2V_t)}C_L^2 V_{dd}^2$$

with a trade-off appearing: as the input capacitance increases, the nergy dissipated in charging the load decreases, but the energy dissipated in charging the inputs increases proportionately.



# Adiabatic amplifier

- Assuming Cn as a free parameter, the minimal energy dissipation is achieved at

$$C_{n_{opt}} = \sqrt{\frac{2\xi}{\alpha T}\frac{Kn}{(V_{dd} - 2V_t)}}C_L$$

Which yields to

$$E_{total_{min}} = 2\alpha C_{n_{opt}} V_{dd}^2 = \sqrt{\frac{8\alpha\xi}{T}\frac{Kn}{(V_{dd} - 2V_t)}}C_L V_{dd}^2$$

The equation shows that switching energy in adiabatic charging scales only to $T^{-1/2}$, instead of to $T^{-1}$ as shown in equation (1).

- In order to improve the result, amplifier stages can be cascaded, with switching energy improvements of $T^{-1/2}$ at each stage. However, parasitic capacitances limit the result in practice.
- So, the cost of using conventionally driven inputs with adiabatic logic is a scaling in switching energy which decreases sublinearly with increases in switching time.



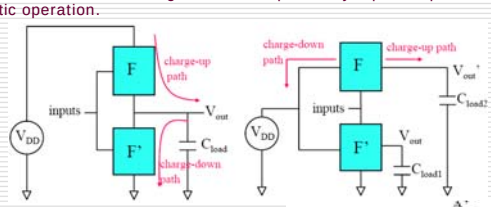
# Adiabatic circuits

## Adiabatic logic circuits

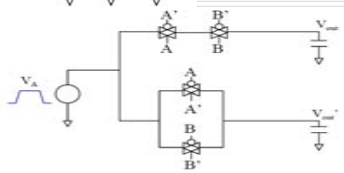
- Adiabatic amplifier extension allows to implement adiabatic charging arbitrary combinational logic functions

### From adiabatic amplifier to adiabatic switched circuit

- Expanded pull-up network to to charge the true output and expanded pull-down network for the complement output.
- The dc Vdd source of the original circuit replaced by a pulsed-power source to allow adiabatic operation.




**An adiabatic CMOS and / nand gate**



# Adiabatic circuits

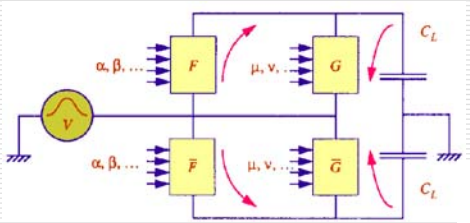
## A pipeline adiabatic gate

- For reasons of performace and complexity management it is desirable to partition a large block of logic into smaller ones and then to compose then to obtain the logic function.
- But adiabatic operation only is possible if the inputs of a gate are held stable while the gate is energized. And a cascade of initially de-energised circuits may be energysed in succesion and then de-energysed in reverse order before the inputs to the cascade may change. This retractile cascades are impractical:
  - the inputs require large and indeterminated number of voltage supplies waveforms
  - waveforms all have different pulse widths
  - since there are N stages, latency is proportional to N but throughput to 1/N
- Pipelining can be used to improve the throughput of the system. If each combinational logic block is replaced by two, one for chargind the output and one for discharging, the inputs may change while the outputs is valid. The inputs for the discharge block must then be driven by the outputs of the following pipeline stage. The stages can be sequenced by overlapping clock signals, which also supply energy to the circuits, to implement reversible pipelines.
  - The logic overhead is approximately a factor of two because of the need for separate charge and discharge blocks, but each path is used once for each full compute cycle because blocks are activated at different time
  - Hence, the energy dissipation is comparable to that of a single block which is used for charging in both directions.

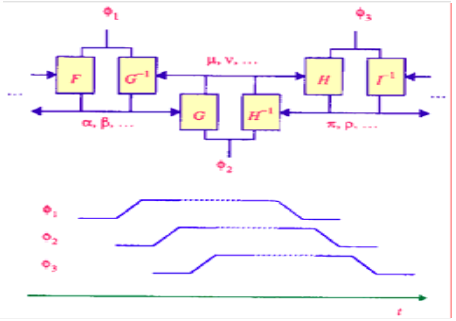


# Adiabatic circuits

## A pipelined adiabatic gate




- The inputs α, β, ... control the F paths through which one of the load capacitances is charged. The G paths, used for discharge, are controlled by a different set of signals: μ, ν, .... In figure, arrows indicates charge flow.



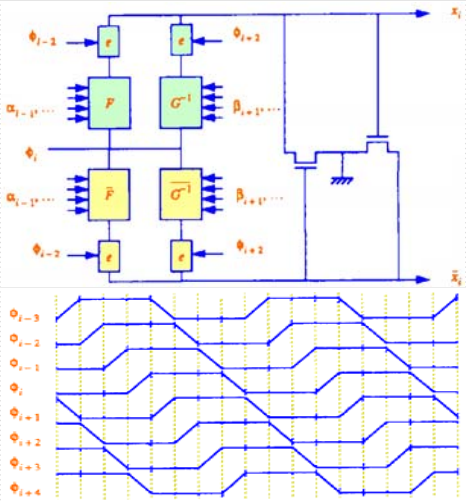

- By constructing all the logic gates according to last figure and restricting the function blocks to invertible functions only, it is possible to assemble a fully adiabatic pipeline.

Conceptual adiabatic pipeline using invertible functions (not shown the multiple switch networks needed for multirail signaling). The corresponding pulse- power/clock signals are shown. One stage must be completely energised before the charge of the next stage starts.

Reversely logic: if the clocks are reversed in time, the pipeline runs backwards.



# Adiabatic circuits




## Detailed dual logic gate for use in reversible pipeline

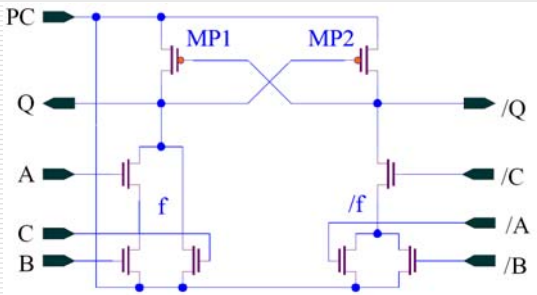
- The gate has 8 phase adiabatic clock signal.
- The enable switches (e) are transmission gates, tied when the indicated clock signal is high.
- For data signals (α,β), the subsignal indicates phase of validity.
- The clamp devices at the output of the gate unsures that the undriven output stays at ground.
- This gate style was used for a highly pipelined FIR filter



# Adiabatic circuits

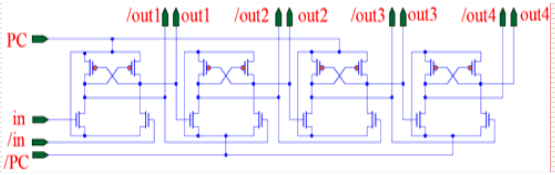
## Measurements in a Dual rail Adiabatic Logic gate (PAL)

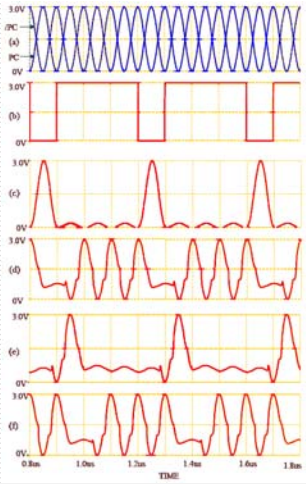
- The PAL gate: true and complementary passtransistor NMOS functional blocks, with a cross-coupled CMOS latch.
  - Power supplied through a sinusoidal power clock (PC)
  - Input states of one of the functional blocks start conducting when PC starts rising from low, while the other remain in tri-state and kept close to 0V by its node capacitance
  - Output state valid around the top of the power clock
  - When power clock ramp down towards zero, energy stored in the output node capacitance is recovered



# Adiabatic circuits

- A 4-stage cascade of PAL inverters
  - Cascade of logic gates is provided by alternate of their power clock ports to PC and 180º phase shifted PC.
  - Odd logic stages are supplied by the sinusoidal voltage PC, while even logic stages are supplied by the shifted PC signal.
  - Logic operation has two phases: evaluate (E), when the power clock is ramping up, and discharge (D), at which power clock ramps down.



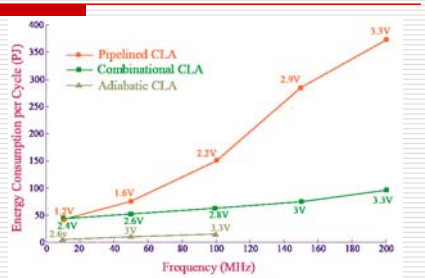




- Simulation results:
  - B) Input of 1st stage
  - C) Output of 1sr stage
  - D) Output of 2nd stage
  - E) Output of 3rd stage
  - F) Output of 4th stage
  - A) Power clock signal



# Adiabatic circuits

- Adder design (CLA)
  - Comparison of simulation results of an 8-bit adder




- Energy consumption vs frequency

  Next to data points there is the minimum supply voltage for each design.

- Energy profiles of the adders at 10MHz while operating at the minimum supply voltage

  It shows the energy recycling phenomenon

  Energy consumption of the combinational adder occurs at the times of the input transitions, and energy consumption of the pipelined adder occurs at the active edges of the clock.

  Signals and power supplies change slowly, effectively removing steep spikes from power supply, and hence decreasing switching noise.